

The TDS5 is a low voltage, high current, thin pack disc SCR employing a amplifying gate structure. This thin package provides greater cooling thus maximizing high current performance. The amplifying gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- Plating Rectifiers

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TDS520503DH is a 2000V-5000A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{TAVG}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TDS5	2000	20	5000	50	0	3	
	1800	18					
	1600	16			500us	200ma	12"
	1400	14			(typ.)	(max)	
	1200	12					

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	2000	Volts
Average On-State Current, $T_C=68^\circ\text{C}$	$I_{T(Avg.)}$	5000	A
RMS On-State Current, $T_C=68^\circ\text{C}$	$I_{T(RMS)}$	7854	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	5700	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	8954	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	90,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	84,852	A
Fuse Coordination I^2t , 60Hz	I^2t	3.38E+07	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	3.60E+07	A^2s
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^\circ\text{C}$
Approximate Weight		6.5	lb
		2.95	Kg
Mounting Force		16,000-20,000	lbs
		71.2 - 89.0	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

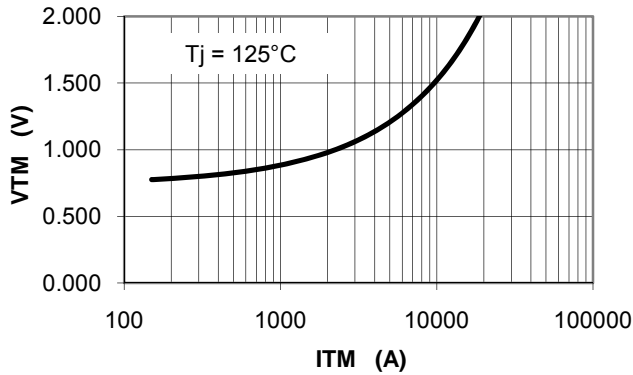
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I_{DRM}	Tj=125°C, V_{DRM} =Rated			200	ma
Repetitive Peak Reverse Leakage Current	I_{RRM}	Tj=125°C, V_{RRM} =Rated			200	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, I_{TM} =4000A			1.15	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.848	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% I_{TM} - $\pi \cdot I_{TM}$			6.58E-02	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			1.117	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			4.74E-02	mΩ
V_{TM} Model, 4-Term	A	Tj=125°C			0.770	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% I_{TM} - I_{TSM}			-0.013	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				3.30E-05	
	D				5.40E-03	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω		4		us
Turn-Off Time	tq	Tj=125°C dv/dt = 20V/us to 67% V_{DRM}			500	us
dv/dt _(crit)	dv/dt	Tj=125°C Exp. Waveform $V_D = 67\%$ Rated	500			V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	150	200	ma
Gate Trigger Voltage	V_{GT}		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

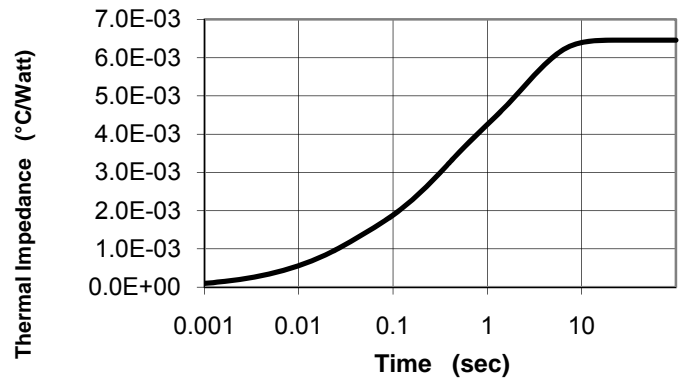
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating				
			max				Units
Thermal Resistance							
Junction to Case	$R\theta_{jc}$	Double side cooled			0.0065	°C/Watt	
Case to Sink	$R\theta_{cs}$	Double side cooled			0.0015	°C/Watt	
Thermal Impedance Model							
$Z\theta_{jc}(t) = \Sigma(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$		Double side cooled					
	where:		N =	1	2	3	4
			A(N) =	1.43E-04	9.08E-04	2.18E-03	3.23E-03
			Tau(N) =	2.62E-03	2.31E-02	2.50E-01	2.50E+00

Maximum On-State Voltage Drop

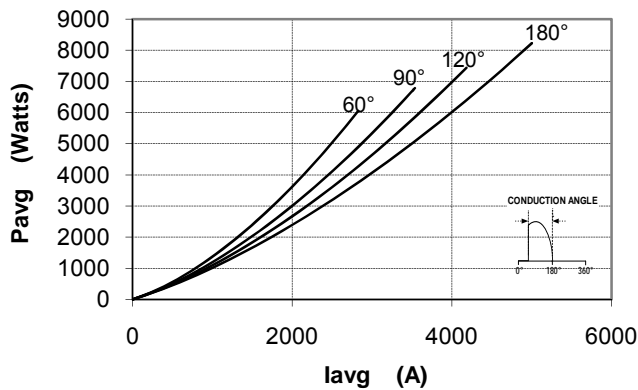


MAXIMUM TRANSIENT THERMAL IMPEDANCE



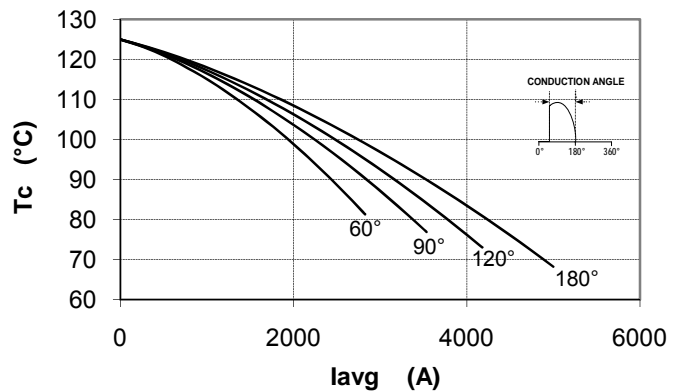
Maximum On-State Power Dissipation

Sinusoidal Waveform



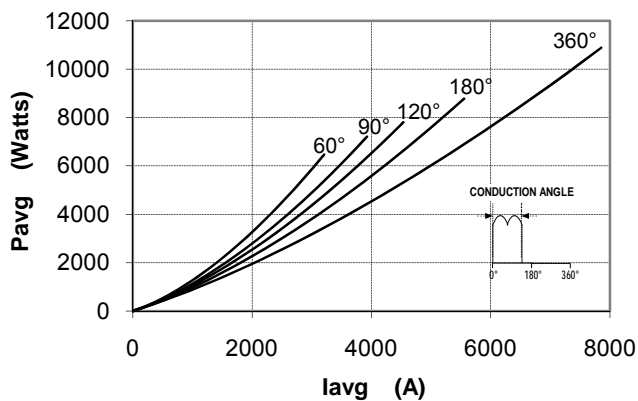
Maximum Allowable Case Temperature

Sinusoidal Waveform



Maximum On-State Power Dissipation

Square Waveform



Maximum Allowable Case Temperature

Square Waveform

