

The TBKD is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- AC Soft-Starters

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TBKD45190HDH is a 4500V - 1890A SCR with 250ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating V _{DRM} -V _{RRM}	Voltage Code	Current Rating I _{tavg}	Current Code	Turn-Off T _q	Gate I _{GT}	Leads
TBKD	4500	45	1890	19	0	H	
	4200	42					
	4000	40			600us (typ.)	250ma (max)	12"

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	4000 - 4500	Volts
Average On-State Current, $T_C=70^{\circ}C$	$I_{T(Avg.)}$	1890	A
RMS On-State Current, $T_C=70^{\circ}C$	$I_{T(RMS)}$	2969	A
Average On-State Current, $T_C=60^{\circ}C$	$I_{T(Avg.)}$	2110	A
RMS On-State Current, $T_C=60^{\circ}C$	$I_{T(RMS)}$	3314	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	33,600	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	31,678	A
Fuse Coordination I^2t , 60Hz	I^2t	4.70E+06	A ² s
Fuse Coordination I^2t , 50Hz	I^2t	5.02E+06	A ² s
Critical Rate-of-Rise of On-State Current Repetitive .67•VDRM	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive .67•VDRM	di/dt	200	A/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	°C
Storage Temperature	$T_{Stg.}$	-50 to+150	°C
Approximate Weight		2.5	lb
		1.13	Kg
Mounting Force		9000-10000	lbs
		40 - 44.5	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

Electrical Characteristics, T_j=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I _{DRM}	T _j =125°C, V _{DRM} =Rated			250	ma
Repetitive Peak Reverse Leakage Current	I _{RRM}	T _j =125°C, V _{RRM} =Rated			250	ma
Peak On-State Voltage	V _{TM}	T _j =125°C, I _{TM} =2000A			1.70	V
V _{TM} Model, Low Level	V ₀	T _j =125°C			1.130	V
V _{TM} = V ₀ + r•I _{TM}	r	15% I _{TM} - π•I _{TM}			2.75E-04	Ω
V _{TM} Model, High Level	V ₀	T _j =125°C			1.274	V
V _{TM} = V ₀ + r•I _{TM}	r	π•I _{TM} - I _{TSM}			2.46E-04	Ω
V _{TM} Model, 4-Term	A	T _j =125°C			0.468	
V _{TM} = A + B•Ln(I _{TM}) +	B	15% I _{TM} - I _{TSM}			0.112	
C•(I _{TM}) + D•(I _{TM}) ^{1/2}	C				0.000249	
	D				-0.00253	
Turn-On Delay Time	t _d	V _D = 0.5•V _{DRM} Gate Drive: 40V - 20Ω			3.5	us
Turn-Off Time	t _q	T _j =125°C dv/dt = 20V/us to 80% V _{DRM}			600	us
Reverse Recovery Current	I _{R(Rec)}	T _j =125°C 1500A -10A/us				A
Reverse Recovery Charge	Q _{RR}					uCoul
dv/dt _(Crit)	dv/dt	T _j =125°C Exp. Waveform V _D =80% Rated	1000			V/us
Gate Trigger Current	I _{GT}	T _j =25°C V _D = 12V	30	150	250	ma
Gate Trigger Voltage	V _{GT}		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V _{GRM}				5	V

Thermal Characteristics

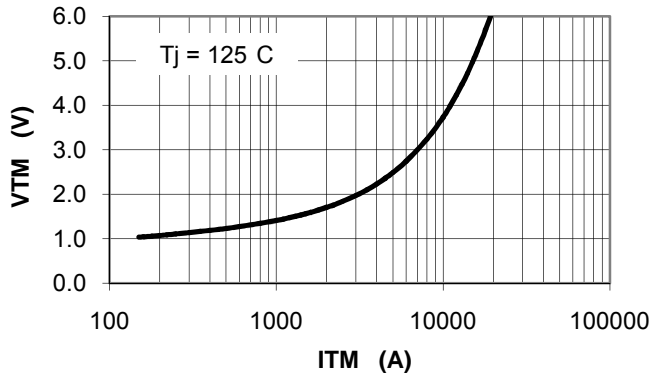
Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	Rθ _{jc}	Double side cooled		0.01	0.012	°C/Watt
Case to Sink	Rθ _{cs}	Double side cooled		0.0015	0.002	°C/Watt

 Thermal Impedance Model Zθ_{jc} Double side cooled

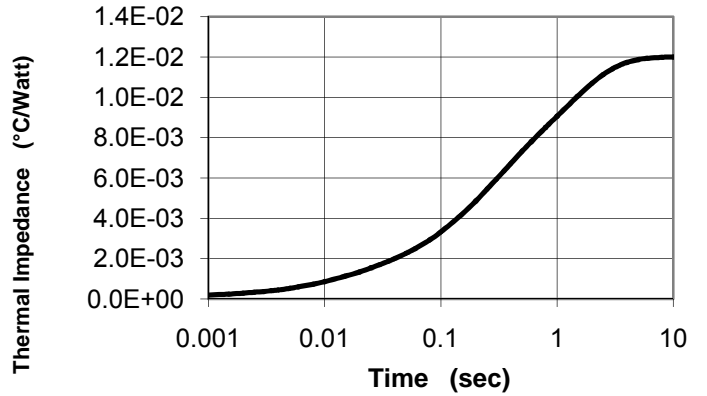
$$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$$

where:	N =	1	2	3	4
	A(N) =	1.10E-04	8.86E-04	4.54E-03	6.47E-03
	Tau(N) =	5.05E-04	1.33E-02	1.95E-01	1.25E+00

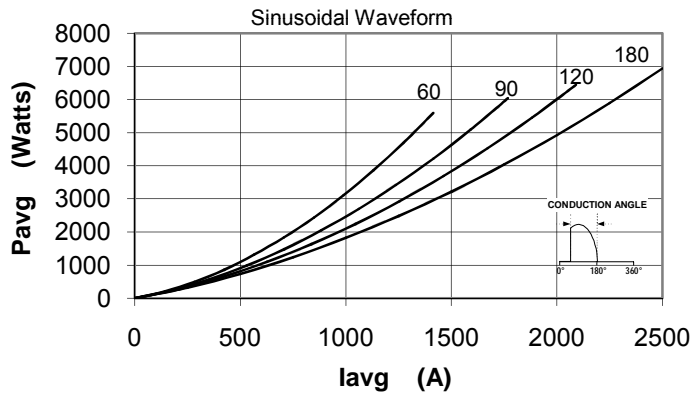
Maximum On-State Voltage Drop



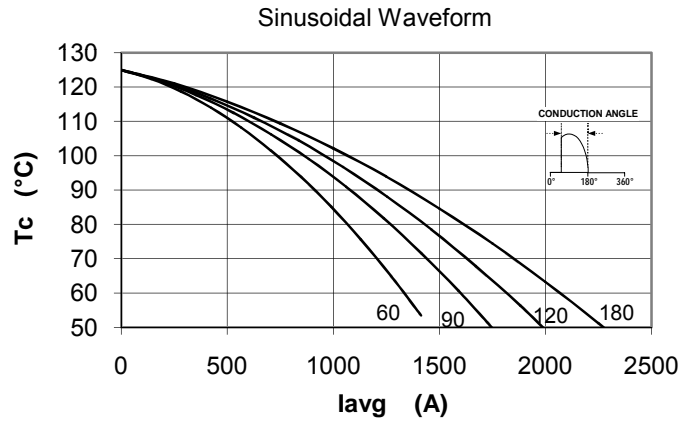
MAXIMUM TRANSIENT THERMAL IMPEDANCE



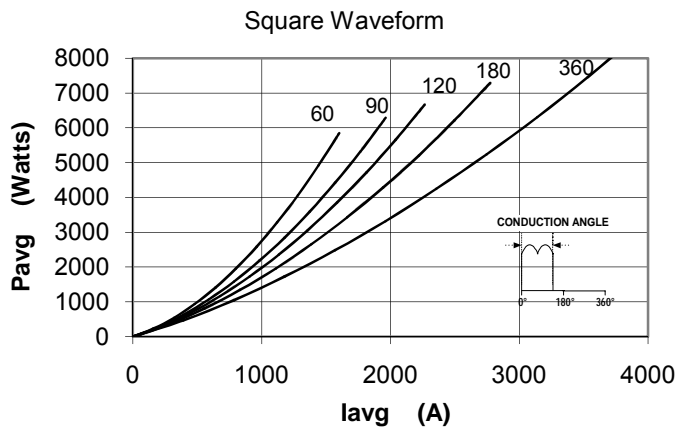
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

