

The TBKC is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I^2t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- AC Soft-Starters

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
EXAMPLE: TBKC651202DH is a 6500V-1200A SCR with 300ma IGT and 12 inch gate and cathode potential leads.

| PART | Voltage Rating $V_{DRM}-V_{RRM}$ | Voltage Code | Current Rating I_{tavg} | Current Code | Turn-Off t_q | Gate I_{GT} | Leads |
|-------------|-------------------------------------|--------------|------------------------------|--------------|-------------------|------------------|-------|
| TBKC | 6500 | 65 | 1250 | 12 | 0 | 2 | |
| | 6200 | 62 | | | | | |
| | 6000 | 60 | | | 800us (typ.) | 300ma (max) | 12" |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

Revised: 12/1/2006

Absolute Maximum Ratings

| Characteristic | Symbol | Rating | Units |
|--|-------------------|------------|------------------|
| Repetitive Peak Voltage | $V_{DRM}-V_{RRM}$ | 6500 | Volts |
| Average On-State Current, $T_C=70^{\circ}C$ | $I_{T(Avg.)}$ | 1250 | A |
| RMS On-State Current, $T_C=70^{\circ}C$ | $I_{T(RMS)}$ | 1963 | A |
| Average On-State Current, $T_C=50^{\circ}C$ | $I_{T(Avg.)}$ | 1500 | A |
| RMS On-State Current, $T_C=50^{\circ}C$ | $I_{T(RMS)}$ | 2356 | A |
| Peak One Cycle Surge Current, 60Hz, $V_R=0V$ | I_{TSM} | 22,000 | A |
| Peak One Cycle Surge Current, 50Hz, $V_R=0V$ | I_{TSM} | 20,742 | A |
| Fuse Coordination I^2t , 60Hz | I^2t | 2.02E+06 | A ² s |
| Fuse Coordination I^2t , 50Hz | I^2t | 2.15E+06 | A ² s |
| Critical Rate-of-Rise of On-State Current | di/dt | 100 | A/us |
| Repetitive .67•VDRM | | | |
| Critical Rate-of-Rise of On-State Current | di/dt | 200 | A/us |
| Non-Repetitive .67•VDRM | | | |
| Peak Gate Power, 100us | P_{GM} | 16 | Watts |
| Average Gate Power | $P_{G(avg)}$ | 5 | Watts |
| Operating Temperature | T_j | -40 to+125 | °C |
| Storage Temperature | $T_{Stg.}$ | -50 to+150 | °C |
| Approximate Weight | | 3.5 | lb |
| | | 1.59 | Kg |
| Mounting Force | | 9000-10000 | lbs |
| | | 40 - 44.5 | KNewtons |

Information presented is based upon manufacturers preliminary testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

Electrical Characteristics, T_j=25°C unless otherwise specified

| Characteristic | Symbol | Test Conditions | Rating | | | Units |
|--|---------------------|--|--------|-----|----------|-------|
| | | | min | typ | max | |
| Repetitive Peak Forward Leakage Current | I _{DRM} | T _j =125°C, V _{DRM} =Rated | | | 400 | ma |
| Repetitive Peak Reverse Leakage Current | I _{RPM} | T _j =125°C, V _{RPM} =Rated | | | 400 | ma |
| Peak On-State Voltage | V _{TM} | T _j =125°C, I _{TM} =2000A | | | 2.75 | V |
| V _{TM} Model, Low Level | V ₀ | T _j =125°C | | | 1.153 | V |
| V _{TM} = V ₀ + r•I _{TM} | r | 15% I _{TM} - π•I _{TM} | | | 7.44E-04 | Ω |
| V _{TM} Model, High Level | V ₀ | T _j =125°C | | | 1.79 | V |
| V _{TM} = V ₀ + r•I _{TM} | r | π•I _{TM} - I _{TSM} | | | 5.60E-04 | Ω |
| V _{TM} Model, 4-Term | A | T _j =125°C | | | 0.000150 | |
| V _{TM} = A + B•Ln(I _{TM}) + | B | 15% I _{TM} - I _{TSM} | | | 0.184 | |
| C•(I _{TM}) + D•(I _{TM}) ^{1/2} | C | | | | 0.000509 | |
| | D | | | | 0.00634 | |
| Turn-On Delay Time | t _d | V _D = 0.5•V _{DRM} Gate Drive: 40V - 20Ω | | | 2.5 | us |
| Turn-Off Time | t _q | T _j =125°C dv/dt = 20V/us to 80% V _{DRM} | | | 800 | us |
| Reverse Recovery Current | I _{R(Rec)} | T _j =125°C 2000A -10A/us | | | 200 | A |
| Reverse Recovery Charge | Q _{RR} | | | | 2800 | uCoul |
| dv/dt _(Crit) | dv/dt | T _j =125°C Exp. Waveform V _D =80% Rated | | | 1000 | V/us |
| Gate Trigger Current | I _{GT} | T _j =25°C V _D = 12V | 40 | 175 | 300 | ma |
| Gate Trigger Voltage | V _{GT} | | 0.8 | 2.0 | 5.0 | V |
| Peak Reverse Gate Voltage | V _{GRM} | | | | 5 | V |

Thermal Characteristics

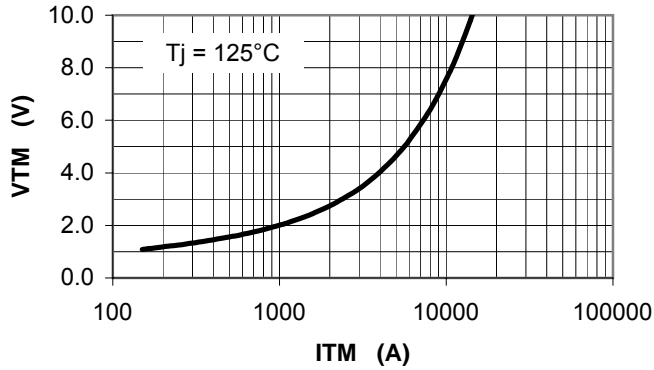
| Characteristic | Symbol | Test Conditions | Rating | | | Units |
|--------------------|------------------|--------------------|--------|--------|-------|---------|
| | | | min | typ | max | |
| Thermal Resistance | | | | | | |
| Junction to Case | Rθ _{jc} | Double side cooled | | 0.0115 | 0.013 | °C/Watt |
| Case to Sink | Rθ _{cs} | Double side cooled | | 0.0015 | 0.002 | °C/Watt |

 Thermal Impedance Model Zθ_{jc} Double side cooled

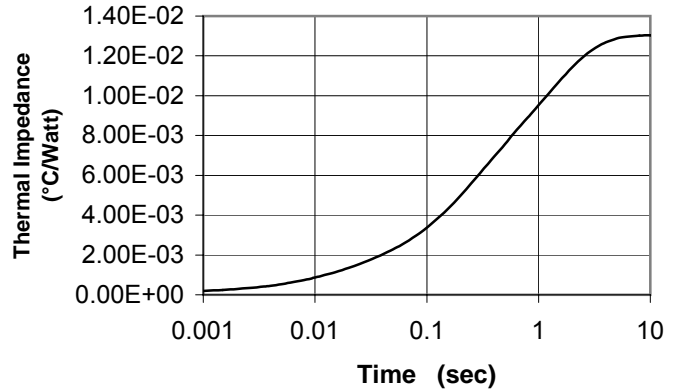
$$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$$

| | | | | | |
|--------|----------|----------|----------|----------|----------|
| where: | N = | 1 | 2 | 3 | 4 |
| | A(N) = | 1.10E-04 | 8.86E-04 | 4.54E-03 | 7.50E-03 |
| | Tau(N) = | 5.05E-04 | 1.33E-02 | 1.95E-01 | 1.30E+00 |

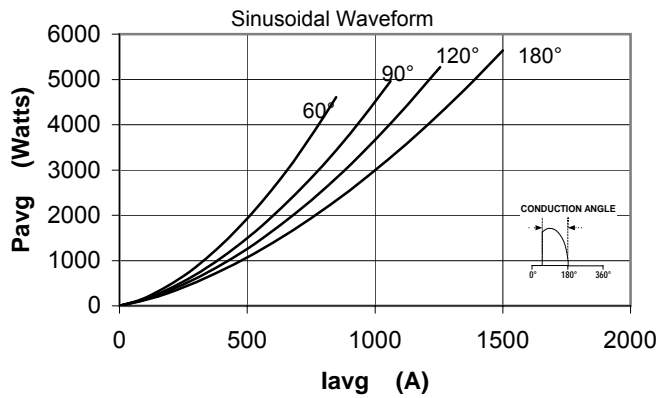
Maximum On-State Voltage Drop



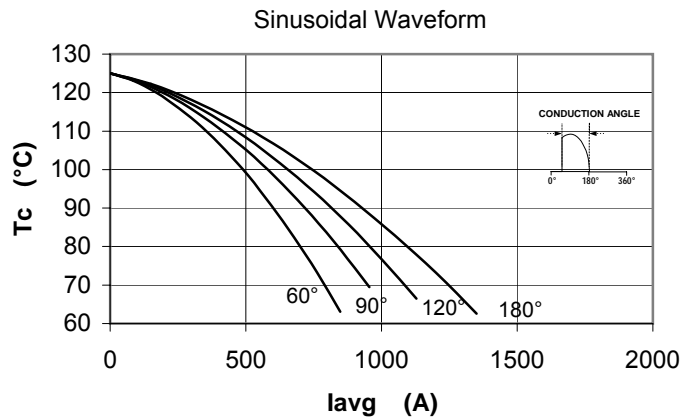
MAXIMUM TRANSIENT THERMAL IMPEDANCE



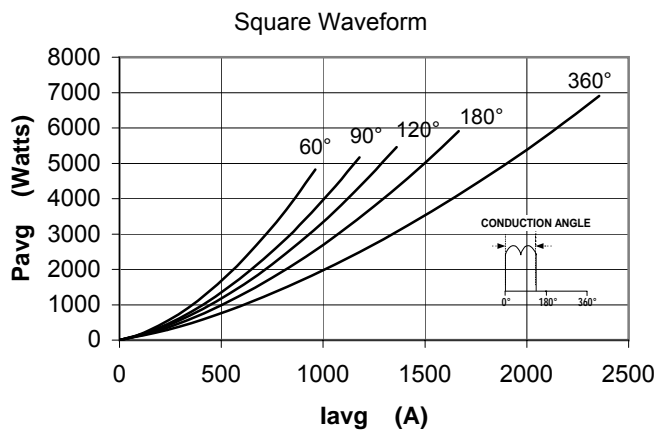
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

