

The TBK5 is a high voltage, high current disc pack SCR employing distributed gate structure. This design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

#### FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and  $I^2t$  Ratings

#### APPLICATIONS:

- DC Power Supplies
- Motor Controls

#### ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.  
 EXAMPLE: TBK5163203DH is a 1600V-3200A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating $I_{TAVG}$	Current Code	Turn-Off $t_q$	Gate $I_{GT}$	Leads
<b>TBK5</b>	800	<b>08</b>	3200	<b>32</b>	<b>0</b>	<b>3</b>	
	1000	<b>10</b>					
	1200	<b>12</b>			400us	200ma	12"
	1400	<b>14</b>			(typ.)	(max)	
	1600	<b>16</b>					

Revised: 9/29/2008

**Absolute Maximum Ratings**

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	1600	Volts
Average On-State Current, $T_C=74^{\circ}C$	$I_{T(Avg.)}$	3200	A
RMS On-State Current, $T_C=74^{\circ}C$	$I_{T(RMS)}$	5027	A
Average On-State Current, $T_C=50^{\circ}C$	$I_{T(Avg.)}$	4100	A
RMS On-State Current, $T_C=50^{\circ}C$	$I_{T(RMS)}$	6440	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	$I_{TSM}$	62,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	$I_{TSM}$	58,454	A
Fuse Coordination $I^2t$ , 60Hz	$I^2t$	1.60E+07	A <sup>2</sup> s
Fuse Coordination $I^2t$ , 50Hz	$I^2t$	1.71E+07	A <sup>2</sup> s
Critical Rate-of-Rise of On-State Current Repetitive $.67 \cdot V_{DRM}$	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive $.67 \cdot V_{DRM}$	di/dt	200	A/us
Peak Gate Power, 100us	$P_{GM}$	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	$T_j$	-40 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		3.5	lb
		1.59	Kg
Mounting Force		9000-10000	lbs
		40 - 44.5	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

**Electrical Characteristics, Tj=25°C unless otherwise specified**

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	$I_{DRM}$	Tj=125°C, $V_{DRM}$ =Rated			150	ma
Repetitive Peak Reverse Leakage Current	$I_{RRM}$	Tj=125°C, $V_{RRM}$ =Rated			150	ma
Peak On-State Voltage	$V_{TM}$	Tj=125°C, $I_{TM}$ =2000A			1.05	V
$V_{TM}$ Model, Low Level	$V_0$	Tj=125°C			0.826	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM}$ - $\pi \cdot I_{TM}$			1.07E-01	mΩ
$V_{TM}$ Model, High Level	$V_0$	Tj=125°C			1.095	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			7.99E-02	mΩ
$V_{TM}$ Model, 4-Term	A	Tj=125°C			0.784	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			-0.016	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				0.000063	
	D				0.00584	
Turn-On Delay Time	$t_d$	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω			3.5	us
Turn-Off Time	$t_q$	Tj=125°C dv/dt = 20V/us to 80% $V_{DRM}$			400	us
Reverse Recovery Current	$I_{R(Rec)}$	Tj=125°C 1500A -10A/us				A
Reverse Recovery Charge	$Q_{RR}$					uCoul
dv/dt <sub>(Crit)</sub>	dv/dt	Tj=125°C Exp. Waveform $V_D$ =80% Rated	1000			V/us
Gate Trigger Current	$I_{GT}$	Tj=25°C $V_D = 12V$	30	100	200	ma
Gate Trigger Voltage	$V_{GT}$		0.8	2.0	3.0	V
Peak Reverse Gate Voltage	$V_{GRM}$				5	V

**Thermal Characteristics**

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	$R\theta_{jc}$	Double side cooled		0.009	0.010	°C/Watt
Case to Sink	$R\theta_{cs}$	Double side cooled		0.0016	0.002	°C/Watt

Thermal Impedance Model  $Z\theta_{jc}$  Double side cooled

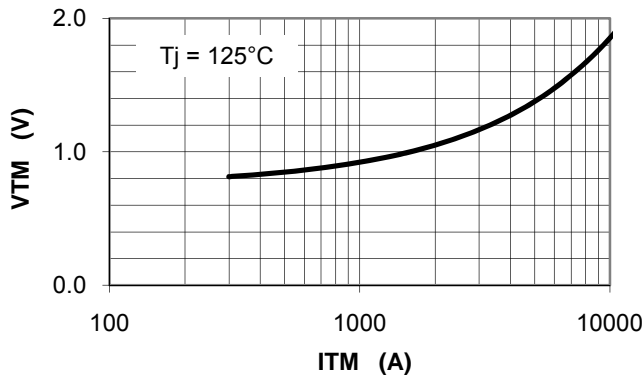
$$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$$

where: N = 1 2 3 4

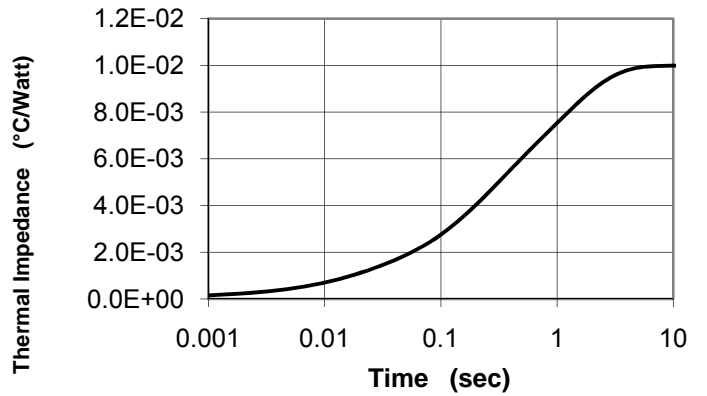
$$A(N) = 1.10E-04 \quad 8.86E-04 \quad 4.54E-03 \quad 4.50E-03$$

$$\text{Tau}(N) = 5.05E-04 \quad 1.33E-02 \quad 2.46E-01 \quad 1.85E+00$$

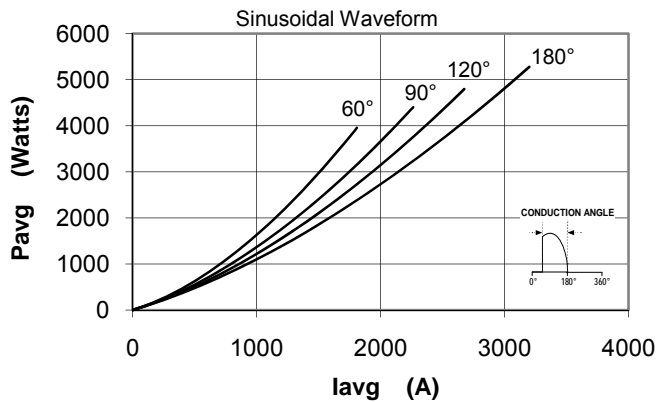
### Maximum On-State Voltage Drop



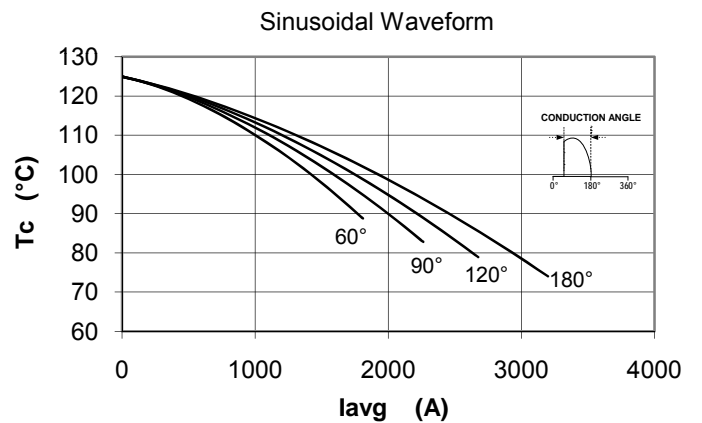
### MAXIMUM TRANSIENT THERMAL IMPEDANCE



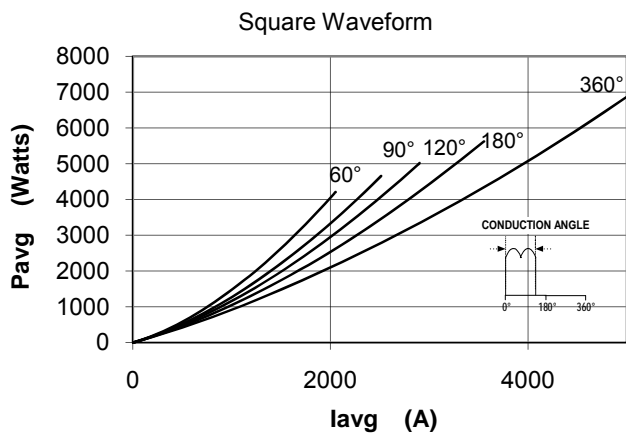
### Maximum On-State Power Dissipation



### Maximum Allowable Case Temperature



### Maximum On-State Power Dissipation



### Maximum Allowable Case Temperature

