

The TAK7 is High Voltage version of the PRX TA20 medium voltage, high current disc pack SCR. It employs a Single-Bar gate, amplifying gate structure. This amplifying gate design allows the SCR to be reliably operated at high di/dt and high dv/dt conditions in phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- AC Soft-Starters

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TAK7321803DH is a 3200V-1800A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{tavg}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TAK7	2400V	24	1800A	18	0	3	DH
	2600V	26					
	2800V	28			550us typ.	200ma	12"
	3000V	30					
	3200V	32					

Revised: 3/26/2010

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	3200	Volts
Non-repetitive Transient Peak Reverse Voltage	V_{RSM}	$V_{RRM} + 100$	Volts
Average On-State Current, $T_C=70^\circ\text{C}$	$I_{T(Avg.)}$	1800	A
RMS On-State Current, $T_C=70^\circ\text{C}$	$I_{T(RMS)}$	2827	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	2100	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	3299	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	23,500	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	22,156	A
Fuse Coordination I^2t , 60Hz	I^2t	2.30E+06	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	2.45E+06	A^2s
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^\circ\text{C}$
Approximate Weight		2.1	lb
		0.95	Kg
Mounting Force		9000 - 11000	lbs
		40.0 - 48.9	Knewtons

Information presented is based upon limited testing or projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

Electrical Characteristics, T_j=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I _{DRM}	T _j =125°C, V _{DRM} =Rated			250	ma
Repetitive Peak Reverse Leakage Current	I _{RRM}	T _j =125°C, V _{RRM} =Rated			250	ma
Peak On-State Voltage	V _{TM}	T _j =125°C, I _{TM} =1500A			1.40	V
V _{TM} Model, Low Level	V ₀	T _j =125°C			0.881	V
V _{TM} = V ₀ + r•I _{TM}	r	15% I _{TM} - π•I _{TM}			3.74E-04	Ω
V _{TM} Model, High Level	V ₀	T _j =125°C			1.11	V
V _{TM} = V ₀ + r•I _{TM}	r	π•I _{TM} - I _{TSM}			3.06E-04	Ω
V _{TM} Model, 4-Term	A	T _j =125°C			0.304	
V _{TM} = A + B•Ln(I _{TM}) +	B	15% I _{TM} - I _{TSM}			0.108	
C•(I _{TM}) + D•(I _{TM}) ^{1/2}	C				1.97E-04	
	D				-6.33E-04	
Turn-On Delay Time	t _d	V _D = 0.5•V _{DRM} Gate Drive: 40V - 20Ω		2.5		us
Turn-Off Time	t _q	T _j =125°C dv/dt = 20V/us to 80% V _{DRM}		550		us
dv/dt _(crit)	dv/dt	T _j =125°C Exp. Waveform V _D =80% Rated	800			V/us
Gate Trigger Current	I _{GT}	T _j =25°C V _D = 12V	50	125	200	ma
Gate Trigger Voltage	V _{GT}		0.8	2.0	4.5	V
Peak Reverse Gate Voltage	V _{GRM}				5	V

Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	Rθ _{jc}	Double side cooled		0.013	0.015	°C/Watt
Case to Sink	Rθ _{cs}	Double side cooled		0.005	0.007	°C/Watt

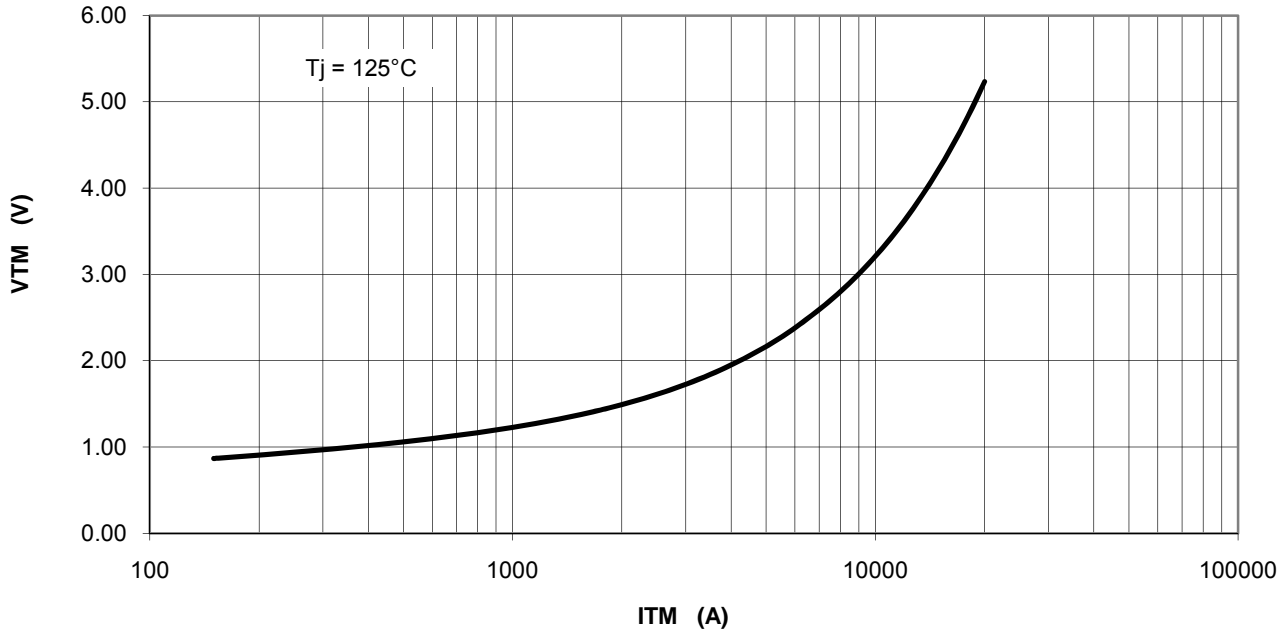
 Thermal Impedance Model Zθ_{jc} Double side cooled

$$Z_{\theta_{jc}}(t) = \sum(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$$

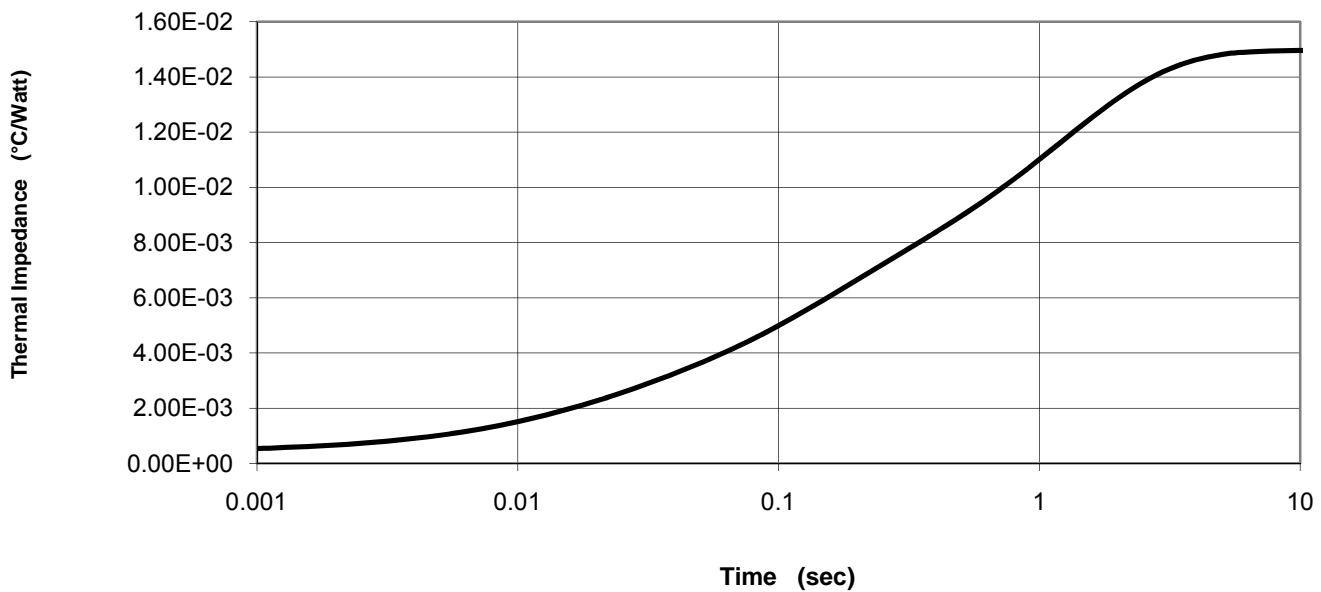
where:

N =	1	2	3	4
A(N) =	4.06E-04	1.40E-03	4.15E-03	9.00E-03
Tau(N) =	9.49E-05	1.52E-02	1.10E-01	1.21E+00

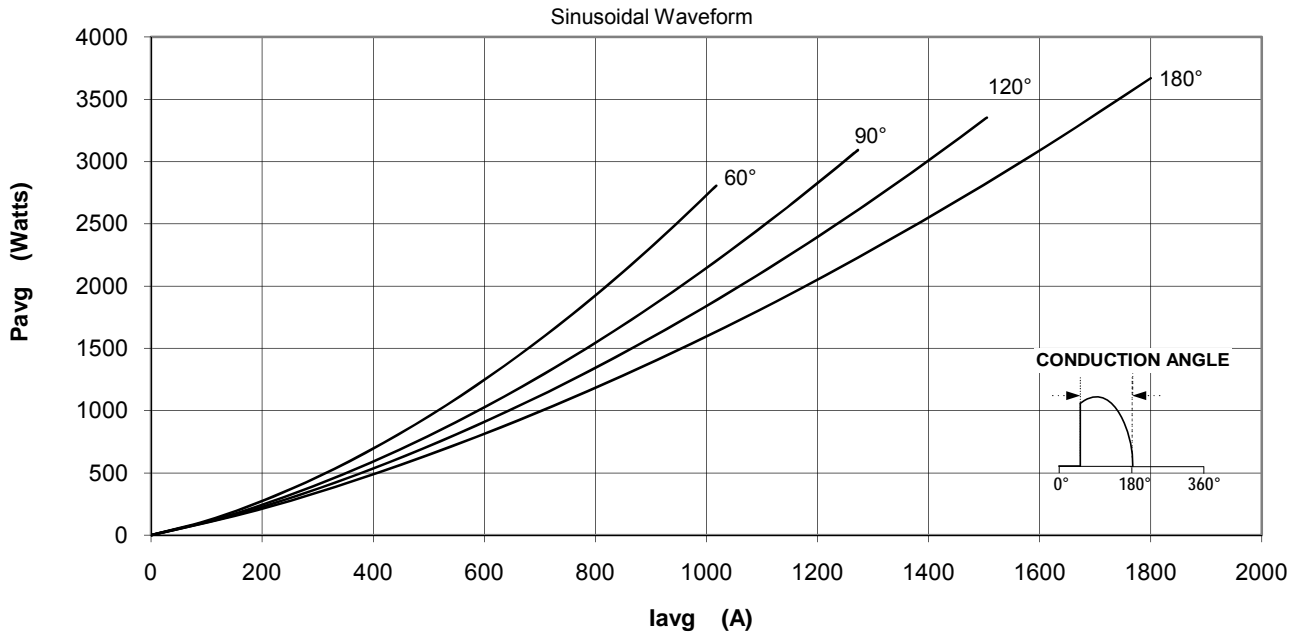
Maximum On-State Voltage Drop



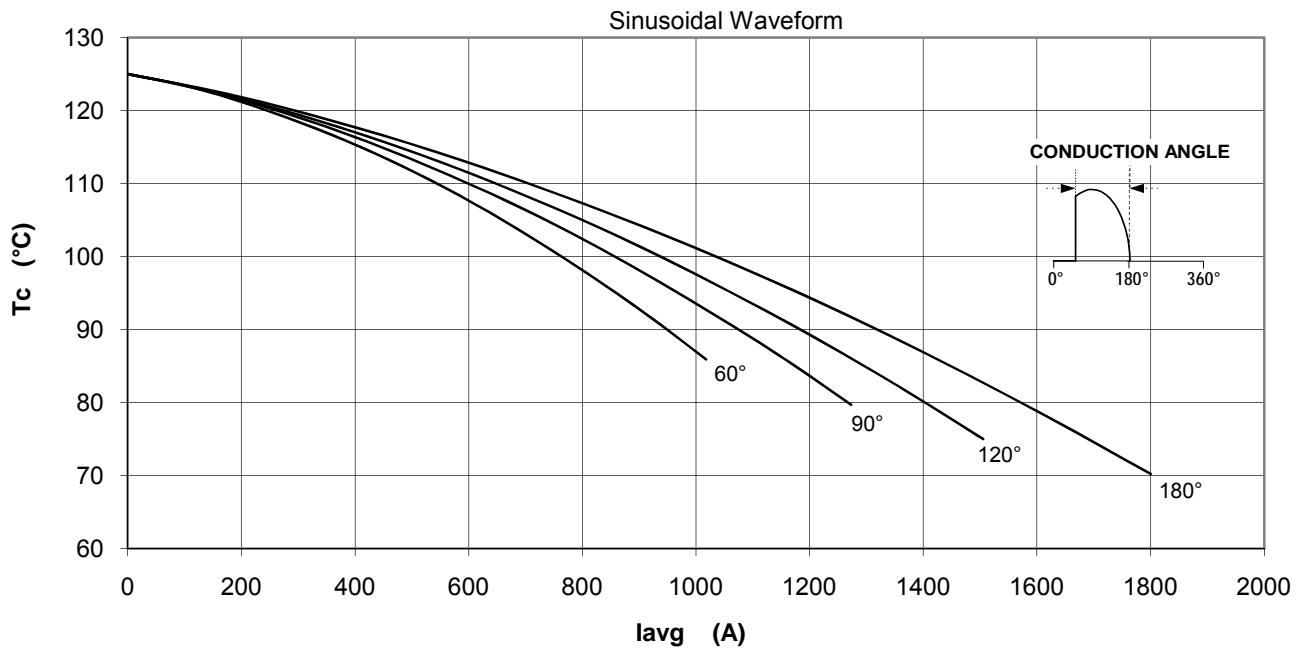
MAXIMUM TRANSIENT THERMAL IMPEDANCE



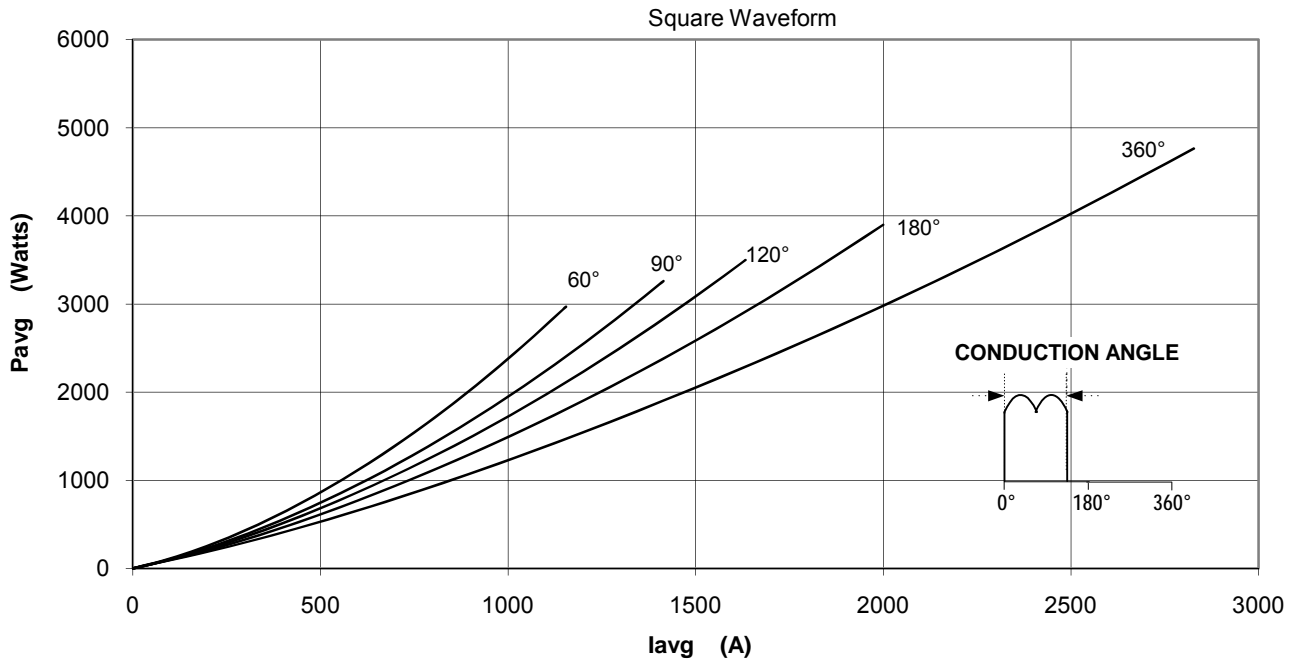
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

