

The T9S0 SCR employs a Center-Fired amplifying gate structure which allows the SCR to be reliably operated at high di/dt and high dv/dt conditions in phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Plating Supplies
- Welding Supplies

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: **T9S0221803DH** is an 2200V-1800A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating V _{DRM} -V _{RRM}	Voltage Code	Current Rating I _{tavg}	Current Code	Turn-Off T _q	Gate I _{GT}	Leads
T9S0	1600V	16	1800A	18	0	3	DH
	1800V	18					
	2000V	20			400us typ.	200ma	12"
	2200V	22					

Revised: 1/6/2009

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	2200	Volts
Average On-State Current, $T_C=70^\circ\text{C}$	$I_{T(Avg.)}$	1800	A
RMS On-State Current, $T_C=72^\circ\text{C}$	$I_{T(RMS)}$	2827	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	1975	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	3102	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	20,600	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	19,422	A
Fuse Coordination I^2t , 60Hz	I^2t	1.77E+06	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	1.89E+06	A^2s
Critical Rate-of-Rise of On-State Current Repetitive	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive	di/dt	200	A/us
Critical Rate-of-Rise of Off-State Voltage $V_D = \frac{1}{2} \cdot V_{DRM}$	dv/dt	1000	V/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-20 to +125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to +150	$^\circ\text{C}$
Approximate Weight		0.65	lb
		0.29	Kg
Mounting Force		5500-6000	lbs
		24.5 - 26.7	Knewtons

Information presented is based upon limited testing or projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

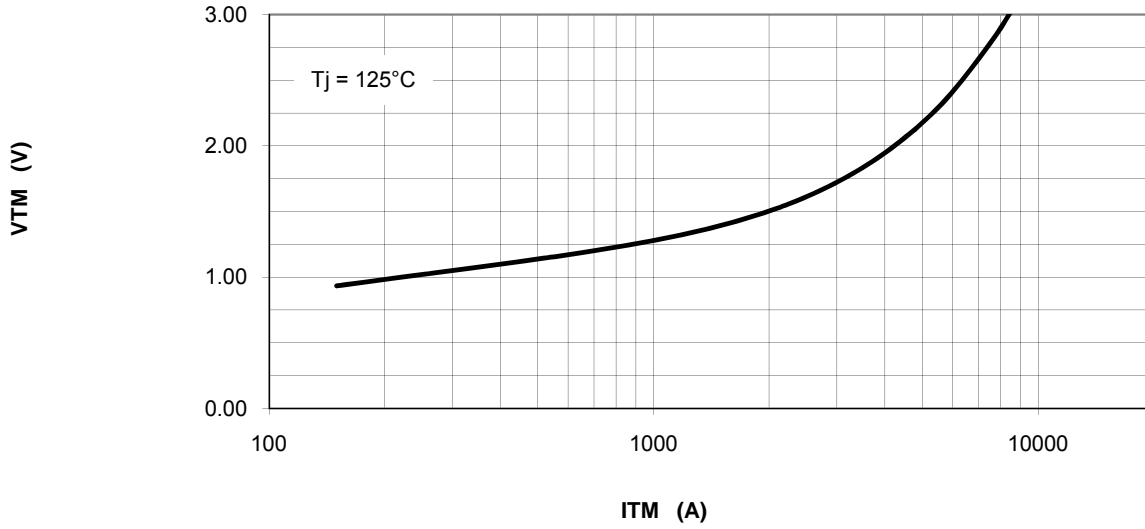
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Leakage Current	I_{DRM}/I_{RRM}	Tj=125°C, V_{DRM} =Rated			150	ma
Peak On-State Voltage	V_{TM}	Tj=25°C, I_{TM} =1500A			1.45	V
V_{TM} Model, Low Level	V_0	Tj=125°C			1.025	V
	$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% I_{TM} - $\pi \cdot I_{TM}$		2.33E-01	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			0.752	V
	$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$		2.65E-01	mΩ
V_{TM} Model, Hiç 4-Term	A	Tj=125°C			-0.149	
	$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$		0.261	
	$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C			3.41E-04	
		D			-2.27E-02	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω		1.5		us
Turn-Off Time	t_q	Tj=125°C $dv/dt = 20V/us$ to 80% V_{DRM}		400		us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	90	200	ma
Gate Trigger Voltage	V_{GT}		0.6	1.6	3.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

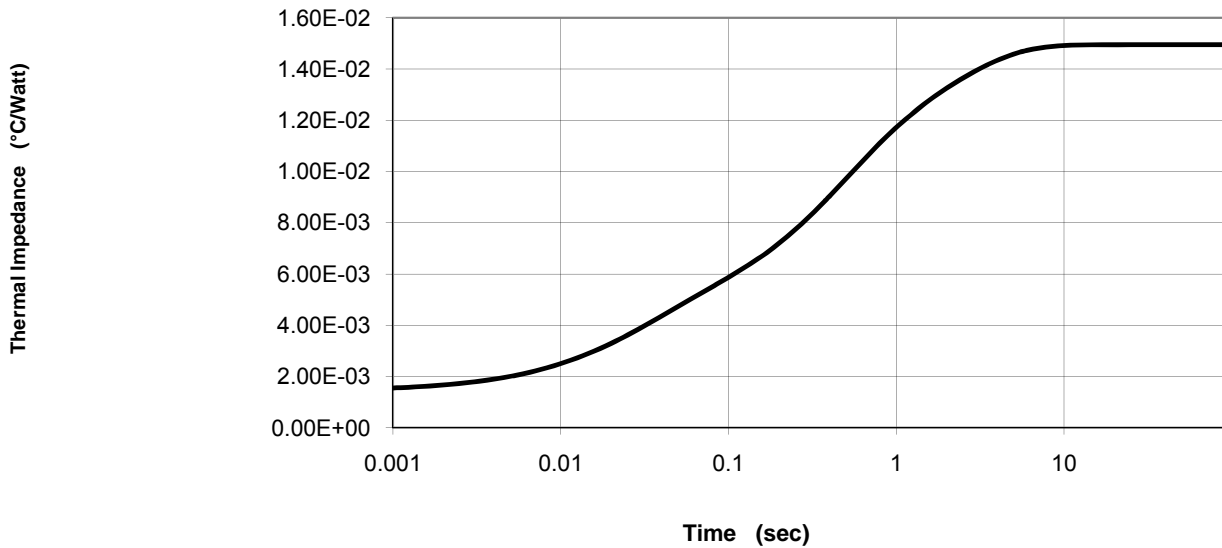
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating																		
			max			Units															
Thermal Resistance																					
Junction to Case	$R\theta_{jc}$	Double side cooled			0.015	°C/Watt															
Case to Sink	$R\theta_{cs}$	Double side cooled			0.0025	°C/Watt															
Thermal Impedance Model																					
	$Z\theta_{jc}$	Double side cooled																			
$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\tau(N))))$ where: <table style="display: inline-table; vertical-align: middle;"> <tr> <td>N =</td> <td>1</td> <td>2</td> <td>3</td> <td>4</td> </tr> <tr> <td>A(N) =</td> <td>1.42E-03</td> <td>2.97E-03</td> <td>6.07E-03</td> <td>4.50E-03</td> </tr> <tr> <td>τ(N) =</td> <td>5.95E-05</td> <td>2.76E-02</td> <td>4.01E-01</td> <td>2.00E+00</td> </tr> </table>							N =	1	2	3	4	A(N) =	1.42E-03	2.97E-03	6.07E-03	4.50E-03	τ(N) =	5.95E-05	2.76E-02	4.01E-01	2.00E+00
N =	1	2	3	4																	
A(N) =	1.42E-03	2.97E-03	6.07E-03	4.50E-03																	
τ(N) =	5.95E-05	2.76E-02	4.01E-01	2.00E+00																	

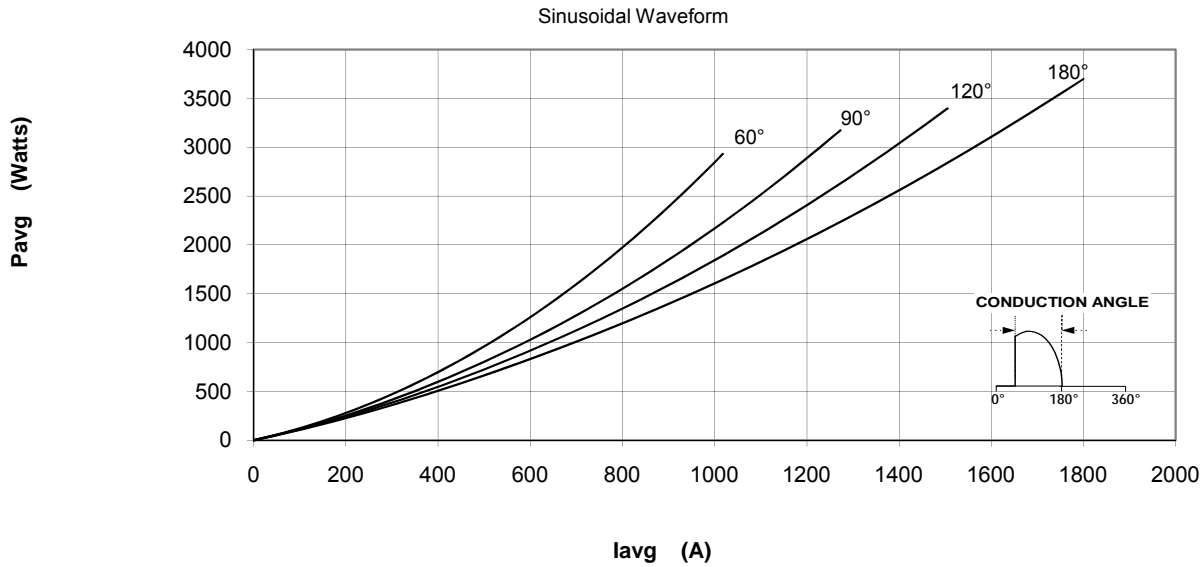
Maximum On-State Voltage Drop



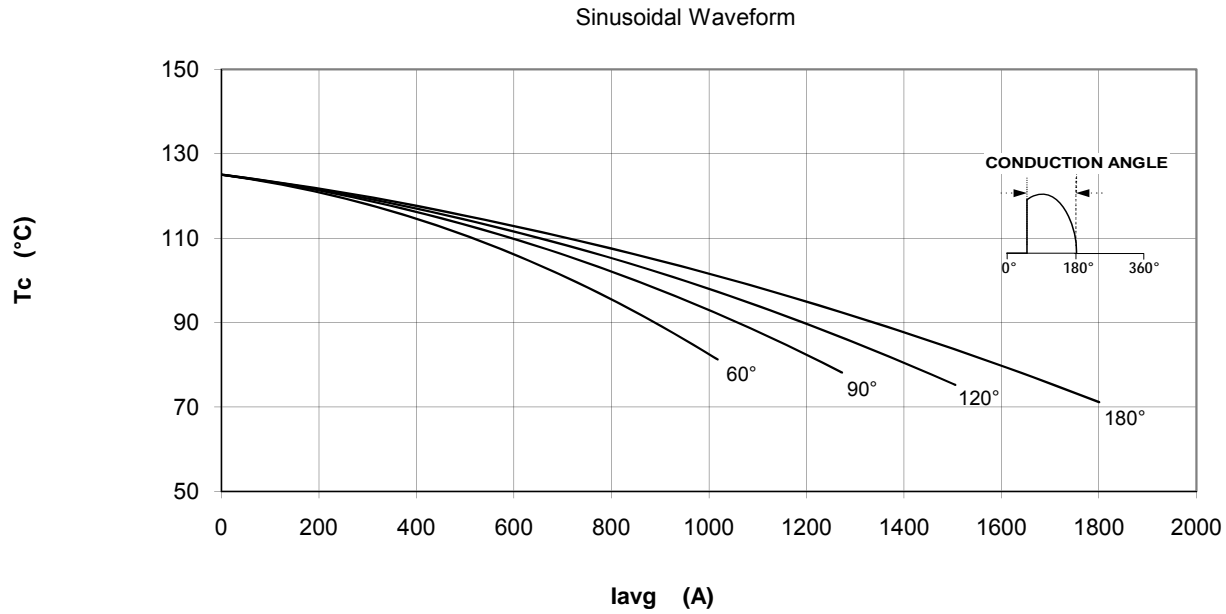
MAXIMUM TRANSIENT THERMAL IMPEDANCE



Maximum On-State Power Dissipation

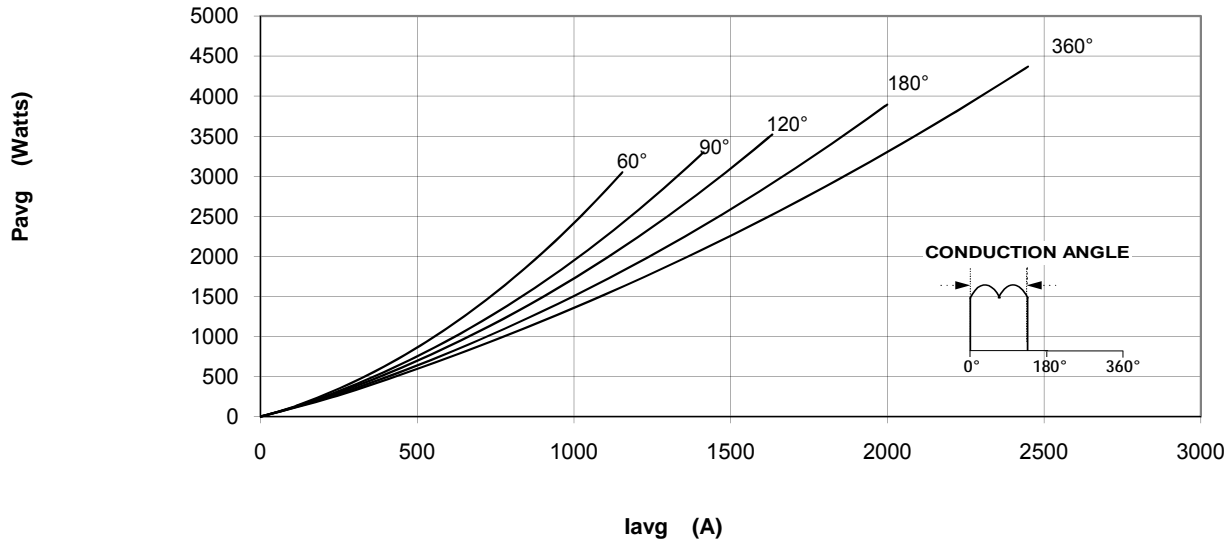


Maximum Allowable Case Temperature



Maximum On-State Power Dissipation

Square Waveform



Maximum Allowable Case Temperature

Square Waveform

