

The T820 is a high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
EXAMPLE: T820188004DH is a 1800V-800A SCR with 150ma I_{GT} and 12 inch gate and cathode potential leads.

PART	Voltage Rating V _{DRM} -V _{RRM}	Voltage Code	Current Rating I _{avg}	Current Code	Turn-Off I _q	Gate I _{GT}	Leads
T820	1800	18	800	80	0	4	DH
	1600	16					
	1400	14			400us (typ.)	150ma (max)	12"

Revised: 5/23/2008

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	1400 - 1800	Volts
Average On-State Current, $T_C=74^{\circ}C$	$I_{T(Avg.)}$	800	A
RMS On-State Current, $T_C=74^{\circ}C$	$I_{T(RMS)}$	1257	A
Average On-State Current, $T_C=55^{\circ}C$	$I_{T(Avg.)}$	1000	A
RMS On-State Current, $T_C=55^{\circ}C$	$I_{T(RMS)}$	1571	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	15,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	14,400	A
Fuse Coordination I^2t , 60Hz	I^2t	9.38E+05	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	1.04E+06	A^2s
Critical Rate-of-Rise of On-State Current Repetitive $.67 \cdot V_{DRM}$	di/dt	100	A/us
Critical Rate-of-Rise of On-State Current Non-Repetitive $.67 \cdot V_{DRM}$	di/dt	200	A/us
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		0.6	lb
		0.27	Kg
Mounting Force		3000-3500	lbs
		13.3 - 15.5	Knewtons

The information on this datasheet is based upon Powerex testing and projected ratings and is subject to change without notice. Powerex makes no implicit or explicit claim to reliability, capability, performance or suitability of this product for a users application. Powerex makes no guarantee of future availability of this product.

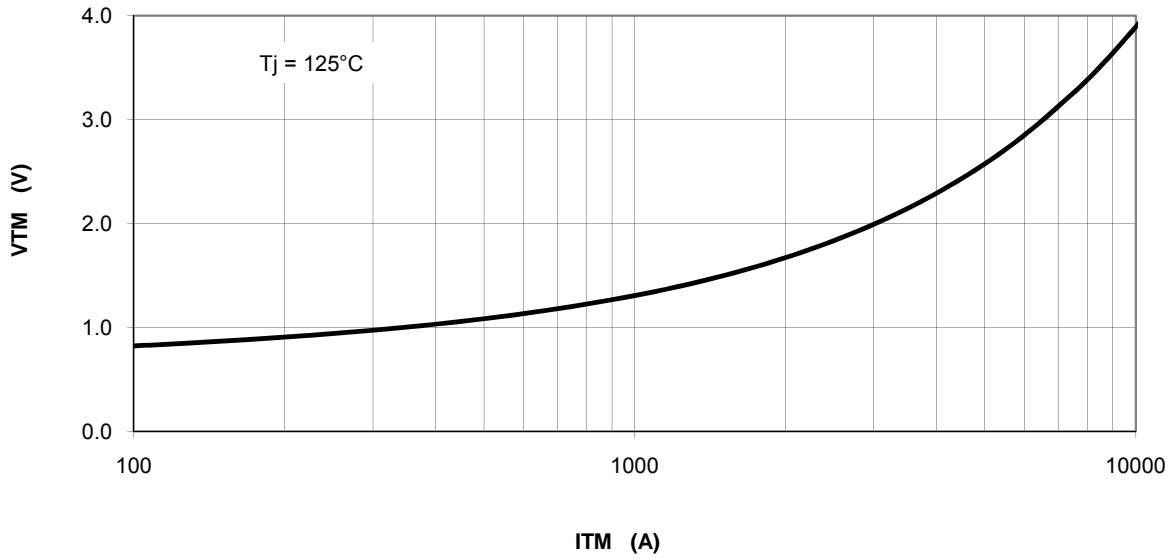
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward/Reverse Leakage Current	I_{DRM} / I_{RRM}	Tj=125°C, $V_{DRM}=V_{RRM}$ =Rated		45	60	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, $I_{TM}=1000A$			1.31	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.893	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - I_{TSM}$			0.386	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			1.24	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			0.262	mΩ
V_{TM} Model, 4-Term	A	Tj=125°C			0.588	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			0.0195	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				1.87E-04	
	D				0.0125	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω		2.0	2.5	us
Turn-Off Time	tq	Tj=125°C dv/dt = 20V/us to 67% V_{DRM}		400	500	us
dv/dt _(crit)	dv/dt	Tj=125°C $V_D = 80\%$ Rated	1000			V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	100	150	ma
Gate Trigger Voltage	V_{GT}		0.8	1.5	3.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V

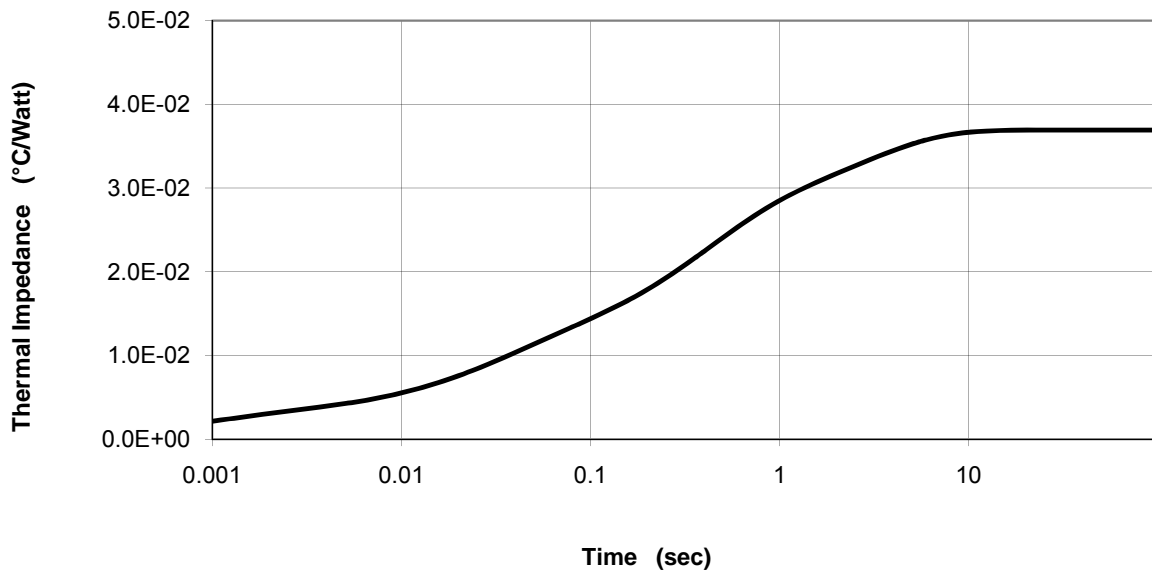
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			Units	
			min	typ	max		
Thermal Resistance							
Junction to Case	$R\theta_{jc}$	Double side cooled			0.037	°C/Watt	
Case to Sink	$R\theta_{cs}$	Double side cooled			0.007	°C/Watt	
Thermal Impedance Model	$Z\theta_{jc}$	Double side cooled					
$Z\theta_{jc}(t) = \Sigma(A(N) \cdot (1 - \exp(-t/Tau(N))))$		where:	N =	1	2	3	4
			A(N) =	2.80E-03	7.59E-03	1.57E-02	1.08E-02
			Tau(N) =	9.30E-04	2.83E-02	3.57E-01	2.69E+00

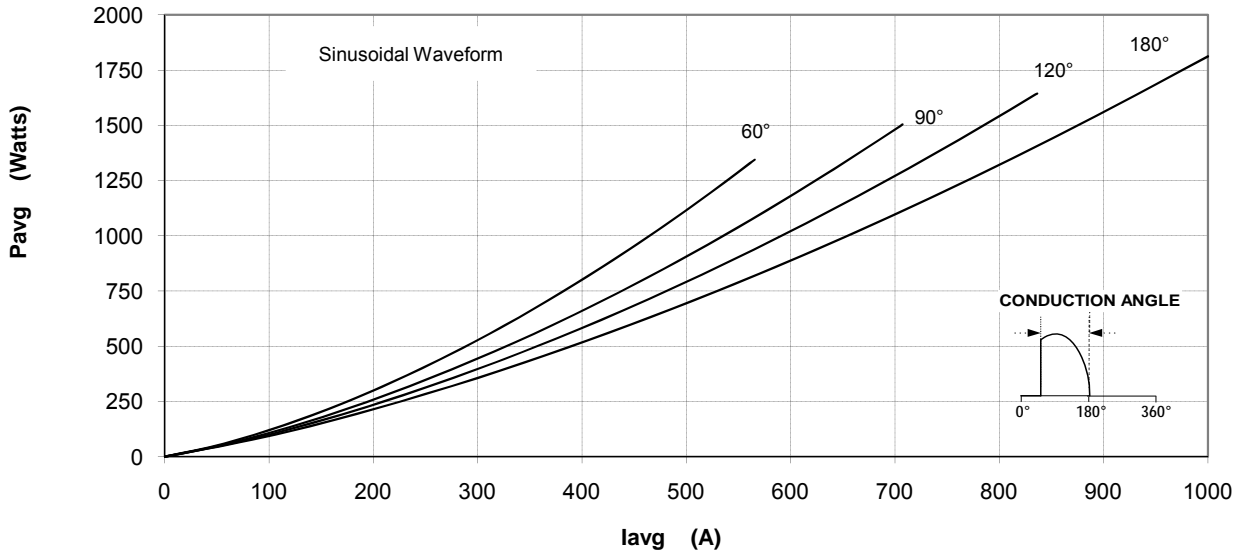
Maximum On-State Voltage Drop



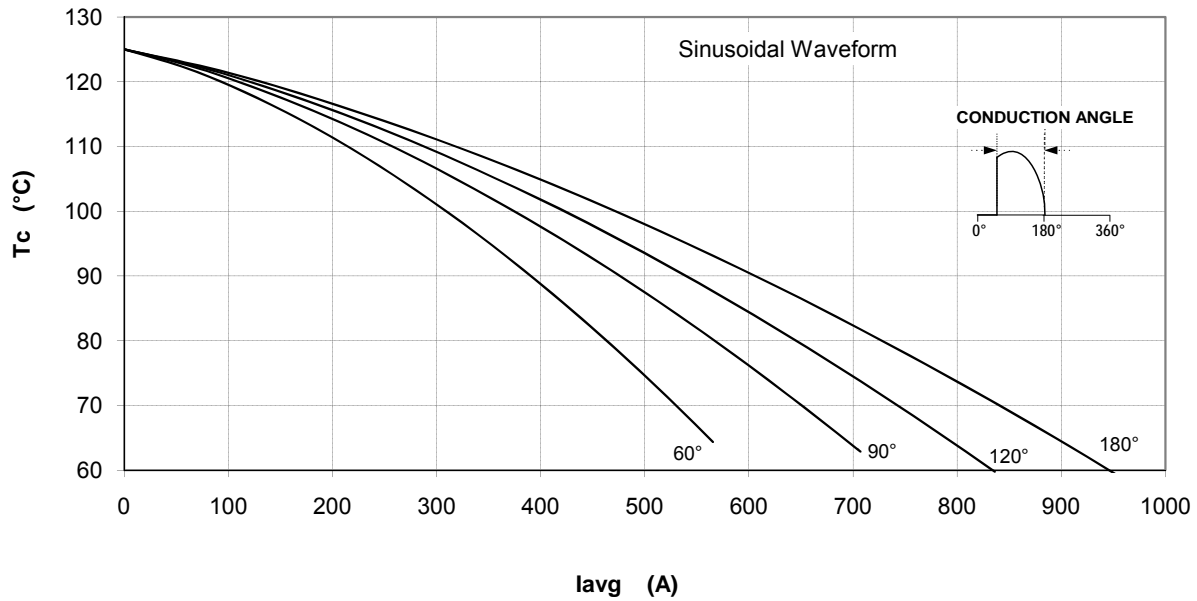
MAXIMUM TRANSIENT THERMAL IMPEDANCE



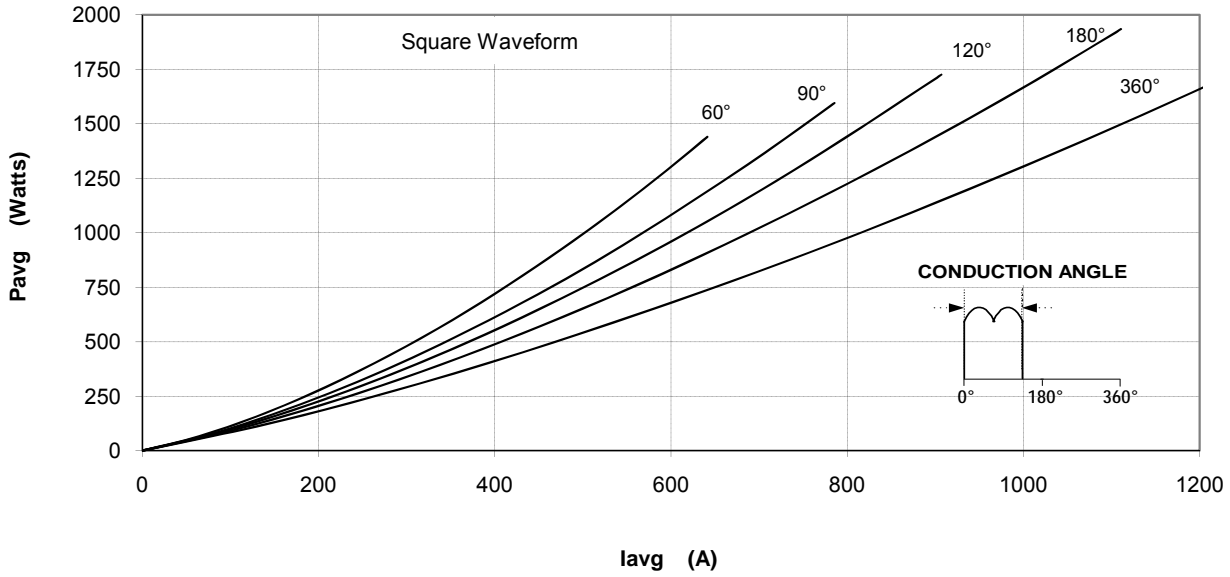
Maximum On-State Power Dissipation



Maximum Allowable Case Temperature



Maximum On-State Power Dissipation



Maximum Allowable Case Temperature

