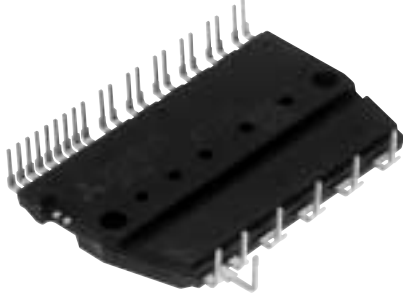


PS21564-SP

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21564-SP



INTEGRATED POWER FUNCTIONS

600V/15A low-loss 5th generation IGBT inverter bridge for three phase DC-to-AC power conversion.
Open emitter type.

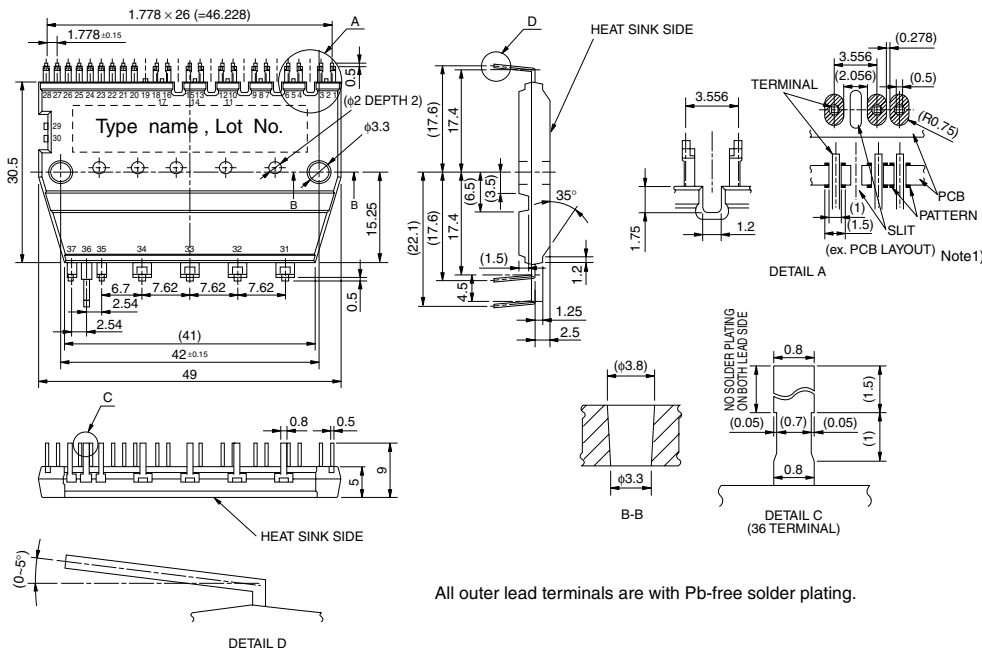
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3,5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES



PS21564-SP

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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-NU, NV, NW	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_f = 25^\circ\text{C}$	15	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_f = 25^\circ\text{C}$, less than 1ms	30	A
PC	Collector dissipation	$T_f = 25^\circ\text{C}$, per 1 chip	22.2	W
T_j	Junction temperature	(Note 1)	-20~+125	$^\circ\text{C}$

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C ($@ T_f \leq 100^\circ\text{C}$) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C}$ ($@ T_f \leq 100^\circ\text{C}$).

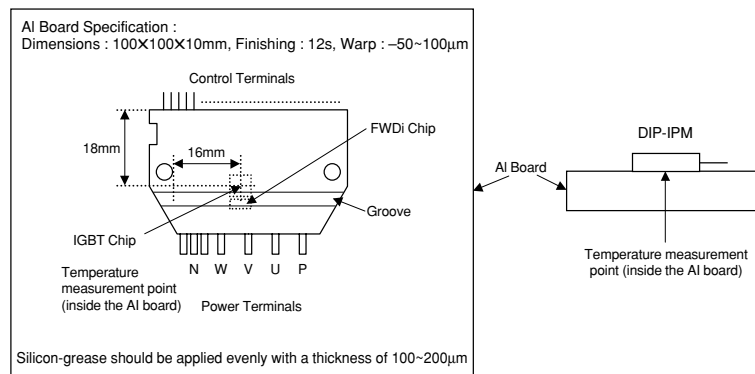
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _f	Module case operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
T _{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V _{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, All connected pins to heat-sink plate	2500	V _{rms}

Note 2 : T_f measurement point



PS21564-SP

TRANSFER-MOLD TYPE
INSULATED TYPE

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-f)Q}	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	4.5	°C/W
R _{th(j-f)F}		Inverter FWD part (per 1/6 module)	—	—	6.5	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V I _C = 15A, T _j = 25°C	—	1.45	1.95	V	
V _{EC}	FWD forward voltage	V _{IN} = 5V I _C = 15A, T _j = 125°C	—	1.55	2.05	V	
t _{on}	Switching times	T _j = 25°C, -I _C = 15A, V _{IN} = 0V	0.60	1.20	1.80	μs	
t _{tr}		V _{CC} = 300V, V _D = V _{DB} = 15V	—	0.30	—	μs	
t _{c(on)}		I _C = 15A, T _j = 125°C, V _{IN} = 0 ↔ 5V	—	0.40	0.60	μs	
t _{off}		Inductive load (upper-lower arm)	—	1.50	2.10	μs	
t _{c(off)}				—	0.50	0.80	μs
I _{CES}		Collector-emitter cut-off current	V _{CE} = V _{CES} T _j = 25°C	—	—	1	mA
		T _j = 125°C	—	—	10		

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit		
			Min.	Typ.	Max.			
I _D	Circuit current	V _D = V _{DB} = 15V V _{IN} = 5V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}		—	5.00	mA	
			V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}		—	0.40		
		V _D = V _{DB} = 15V V _{IN} = 0V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}		—	7.00		
			V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}		—	0.55		
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O circuit pull-up to 5V with 10kΩ	4.9	—	—	V		
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA	—	—	0.95	V		
V _{SC(ref)}	Short circuit trip level	T _f = -20~100°C, V _D = 15V (Note 4)	0.45	—	0.52	V		
I _{IN}	Input current	V _{IN} = 5V	1.0	1.5	2.0	mA		
UV _{DBt}	Control supply under-voltage protection	T _j ≤ 125°C	Trip level		10.0		—	12.0
UV _{DBr}			Reset level		10.5		—	12.5
UV _{Dt}			Trip level		10.3		—	12.5
UV _{Dr}			Reset level		10.8		—	13.0
t _{FO}	Fault output pulse width	C _{FO} = 22nF (Note 5)	1.0	1.8	—	ms		
V _{th(on)}	ON threshold voltage	Applied between UP, VP, WP-V _{NC} , UN, VN, WN-V _{NC}	2.1	2.3	2.6	V		
V _{th(off)}	OFF threshold voltage		0.8	1.4	2.1	V		

Note 4: Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

5: Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure. The fault output pulse width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : C_{FO} = 12.2 × 10⁻⁶ × t_{FO} [F].

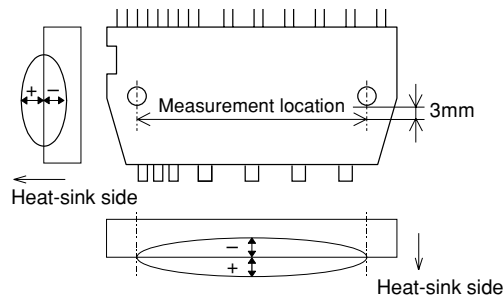
PS21564-SP

TRANSFER-MOLD TYPE
INSULATED TYPE

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	Recommended : 0.78 N·m	0.59	—	0.98	N·m
Weight			—	20	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Recommended value			Unit	
			Min.	Typ.	Max.		
V _{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V	
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	13.5	15.0	16.5	V	
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.0	15.0	18.5	V	
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs	
t _{dead}	Arm shoot-through blocking time	For each input signal, T _r ≤ 100°C	2.0	—	—	μs	
f _{PWM}	PWM input frequency	T _r ≤ 100°C, T _j ≤ 125°C	—	—	20	kHz	
I _O	Allowable r.m.s. current	V _{CC} = 300V, V _D = V _{DB} = 15V, P.F = 0.8, sinusoidal output T _r ≤ 100°C, T _j ≤ 125°C (Note 7)	f _{PWM} = 5kHz	—	—	7.5	Arms
			f _{PWM} = 15kHz	—	—	4.8	
P _{WIN(on)}	Allowable minimum input pulse width	200 ≤ V _{CC} ≤ 350V, 13.5 ≤ V _D ≤ 16.5V, 13.0 ≤ V _{DB} ≤ 18.5V, -20°C ≤ T _r ≤ 100°C, N-line wiring inductance less than 10nH (Note 9)	(Note 8)	0.3	—	—	μs
P _{WIN(off)}			Below rated current	0.5	—	—	
			Between rated current and 1.7 times of rated current	2.0	—	—	
	Between 1.7 times and 2.0 times of rated current	2.6	—	—			
V _N C	V _N C variation	between V _N C-NU, NV, NW (including surge)	-5.0	—	5.0	V	

Note 7: The allowable r.m.s. current value depends on the actual application conditions.

8: The input pulse width less than P_{WIN(on)} might make no response.

9: IPM might not work properly or make response for the input signal with OFF pulse width less than P_{WIN(off)}.

Please refer to Fig.5.

PS21564-SP

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INSULATED TYPE

Fig. 2 THE DIP-IPM INTERNAL CIRCUIT

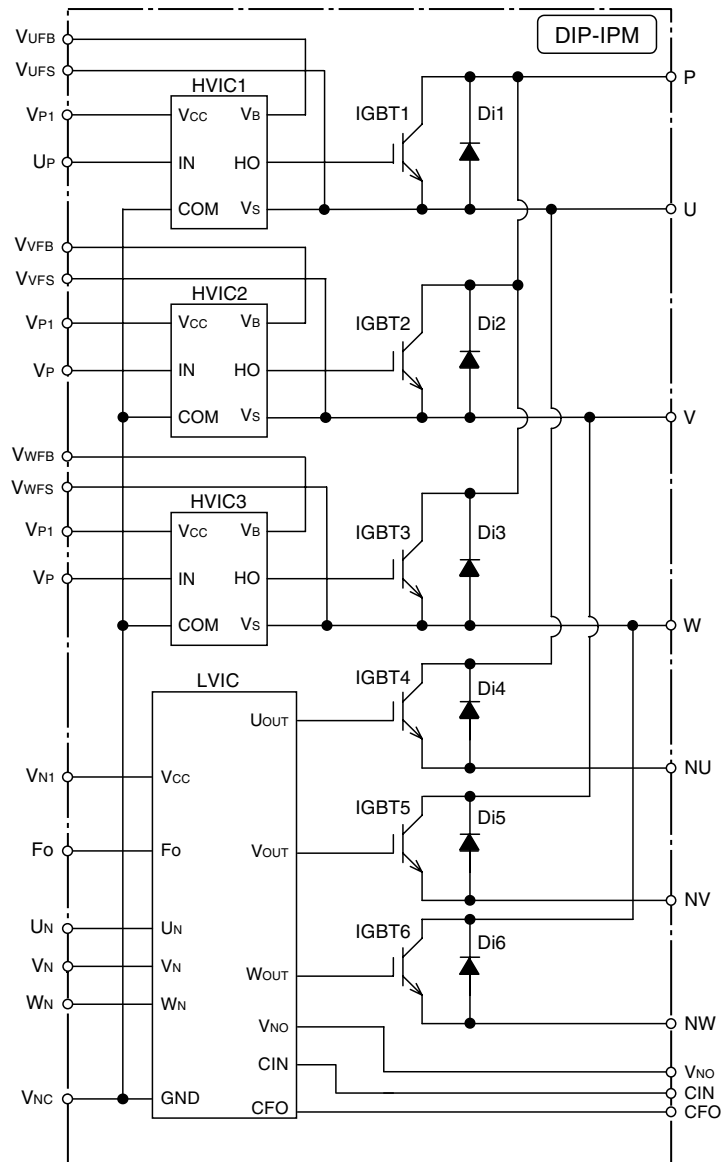
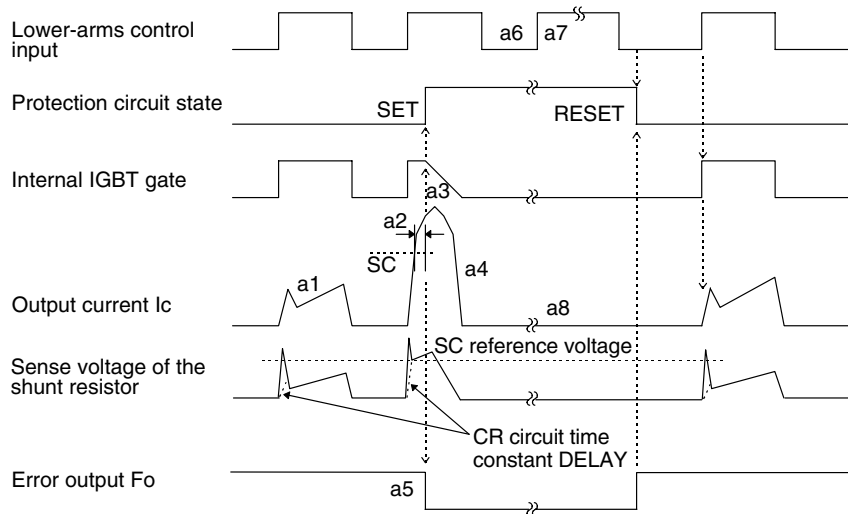


Fig. 3 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

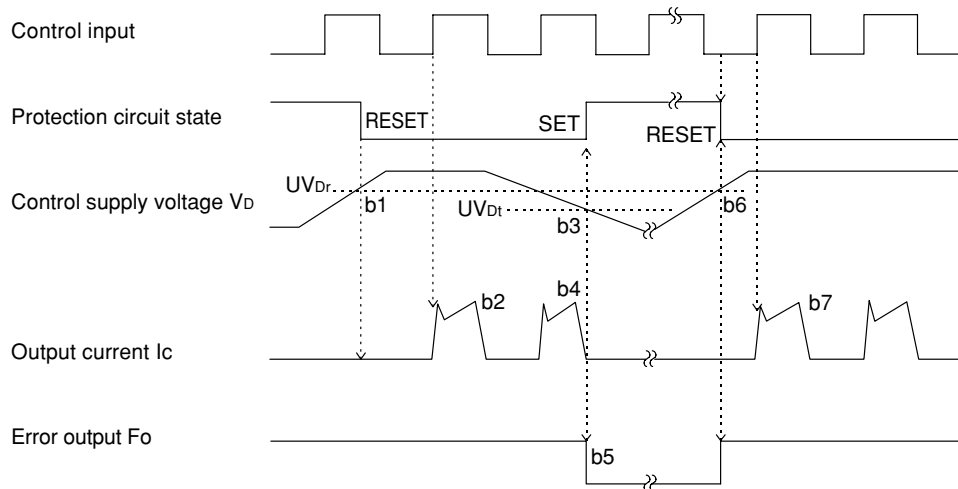
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor C_{FO}.
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UVd)

- b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. FO operation starts.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-arm, UVDB)

- c1. Control supply voltage rises : After the voltage reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

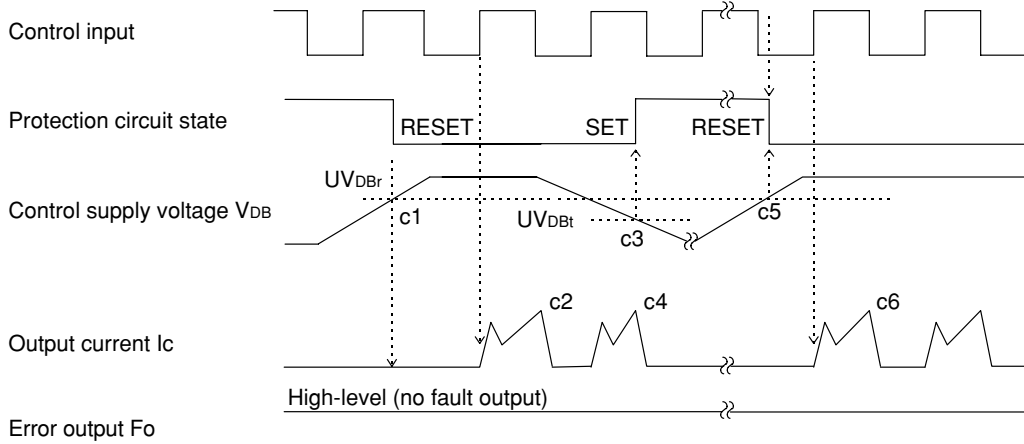
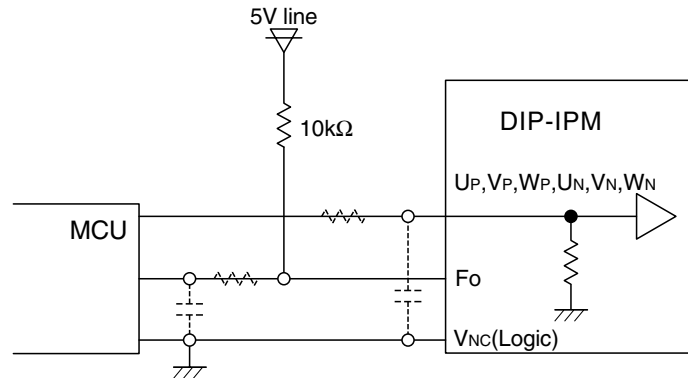


Fig. 4 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
The DIP-IPM input section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 5 WIRING CONNECTION OF SHUNT RESISTOR

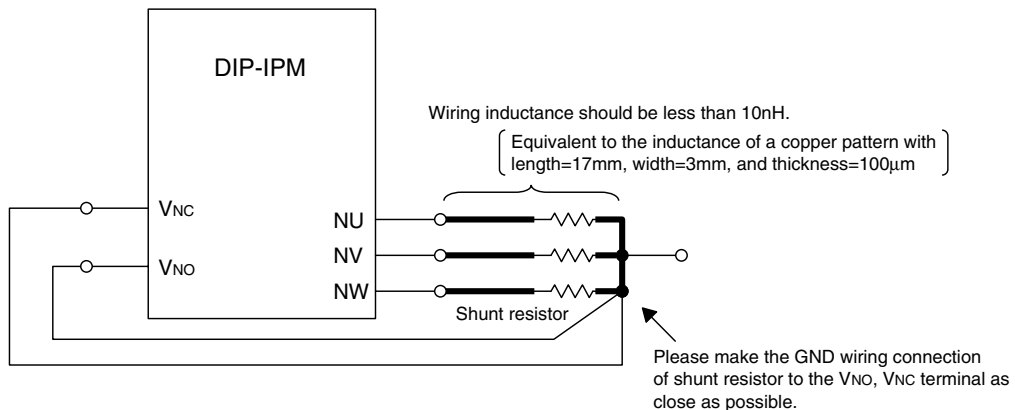
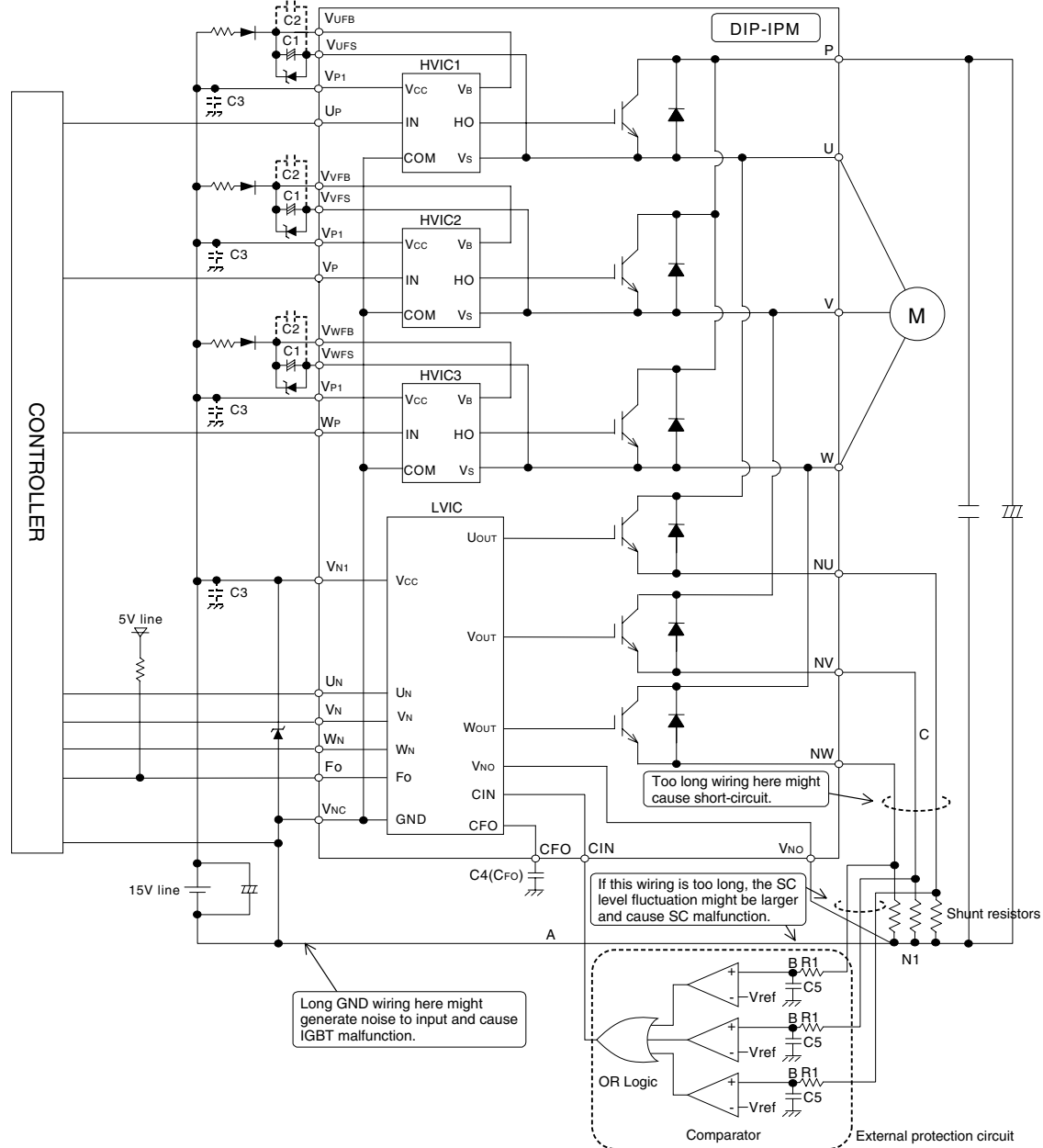


Fig. 6 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE

C1:Tight tolerance temp-compensated electrolytic type C2,C3: 0.22~2μF R-category ceramic capacitor for noise filtering



- Note 1 :** To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)
- 2 :** By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3 :** Fo output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.
- 4 :** Fo output pulse width is determined by the external capacitor between CFO and Vnc terminals (CFO). (Example : CFO = 22 nF → tFO = 1.8 ms (typ.))
- 5 :** The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.
- 6 :** To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.
- 7 :** Please set the C5R1 time constant in the range 1.5~2μs.
- 8 :** Each capacitor should be located as nearby the pins of the DIP-IPM as possible.
- 9 :** To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P-N1 pins is recommended.
- 10 :** To prevent ICs from surge destruction, it is recommended to insert a Zener diode (24V, 1W) between each control supply terminals.
- 11 :** The reference voltage Vref of comparator should be set up the same rating of short circuit trip level (Vsc(ref): min.0.45V to max.0.52V).
- 12 :** OR logic output level should be set up the same rating of short circuit trip level (Vsc(ref): min.0.45V to max.0.52V).