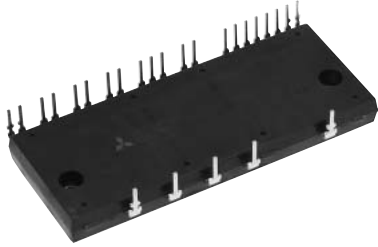


PS21265-P/AP

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21265



INTEGRATED POWER FUNCTIONS

600V/20A low-loss 5th generation IGBT inverter bridge for three phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

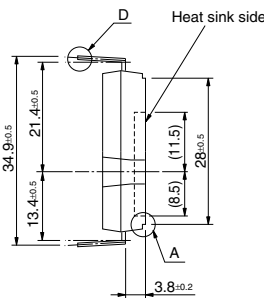
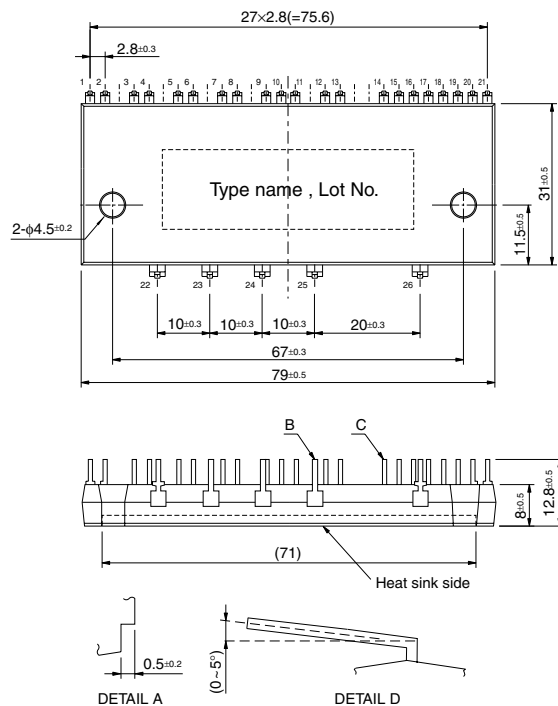
- For upper-leg IGBTs : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 3, 5V line compatible. (High Active)
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (Short-pin type : PS21265-P) Refer Fig. 6 for long-pin type : PS21265-AP.

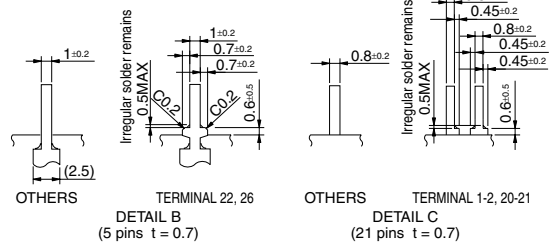
Dimensions in mm



NOTE

TERMINAL CODE

1. UP	14. VN1
2. VP1	15. VNC
3. VUFB	16. CIN
4. VUFS	17. CFO
5. VP	18. FO
6. VP1	19. UN
7. VVFB	20. VN
8. VVFS	21. WN
9. WP	22. P
10. VP1	23. U
11. VPC	24. V
12. VVFB	25. W
13. VVFS	26. N



Note: All outer lead terminals are with Pb-free solder plating.

PS21265-P/AP

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Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

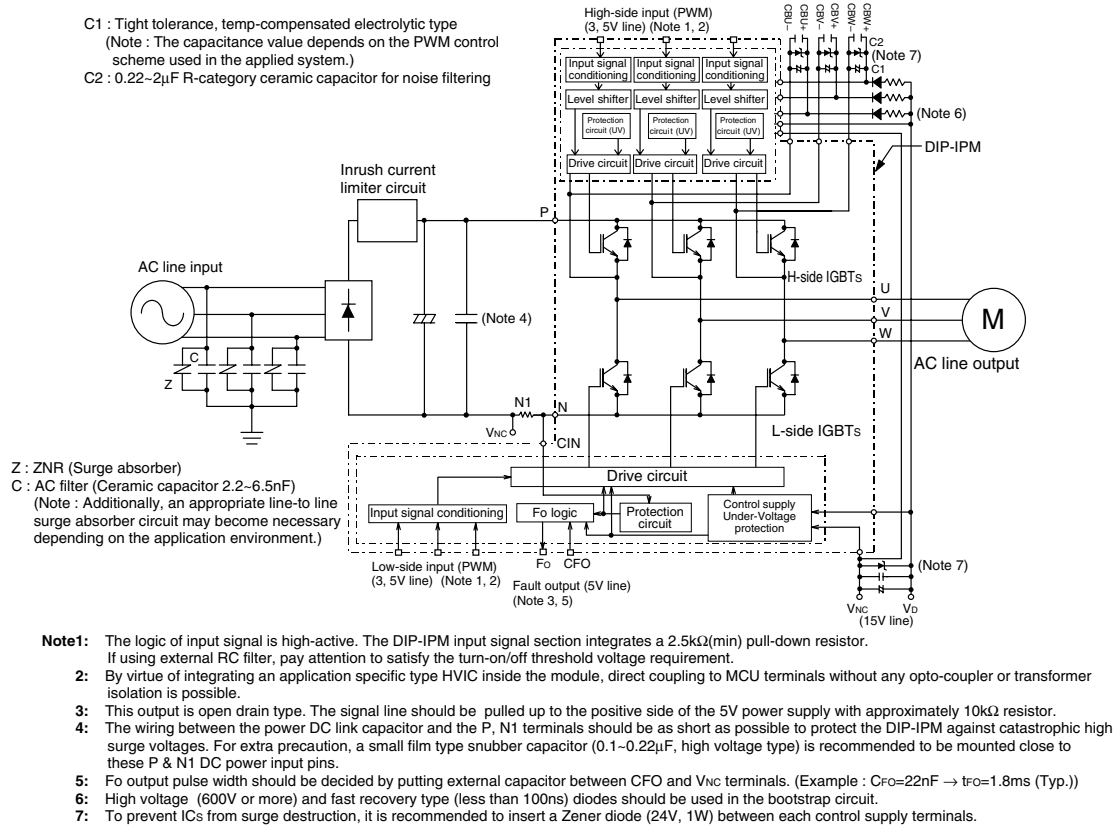
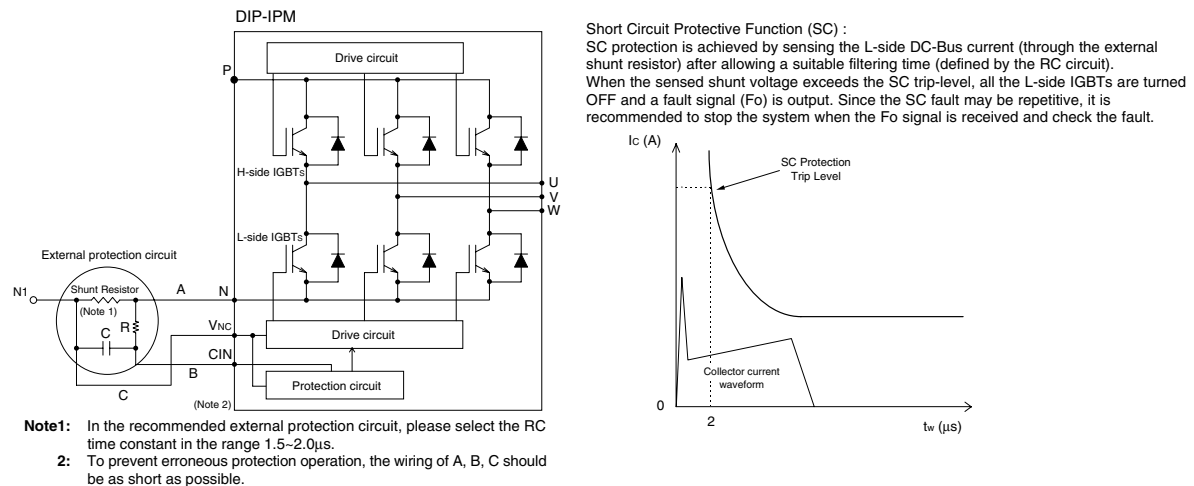


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



PS21265-P/AP

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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_c = 25^\circ\text{C}$	20	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$, less than 1ms	40	A
PC	Collector dissipation	$T_c = 25^\circ\text{C}$, per 1 chip	51.2	W
T_j	Junction temperature	(Note 1)	-20~+125	$^\circ\text{C}$

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_c \leq 100^\circ\text{C}$) however, to insure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C}$ (@ $T_c \leq 100^\circ\text{C}$).

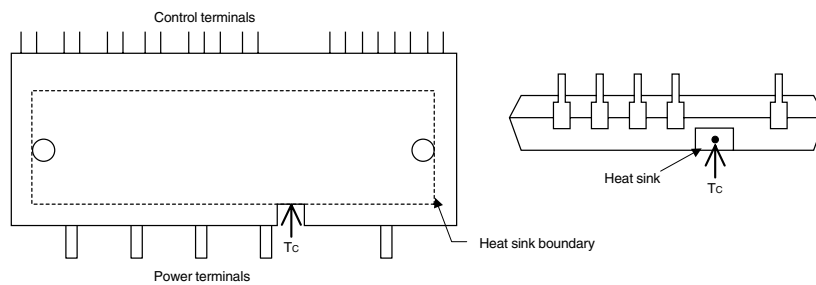
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(Prot)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _c	Module case operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
T _{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connecting pins to heat-sink plate	2500	V _{rms}

Note 2 : T_c measurement point



PS21265-P/AP

TRANSFER-MOLD TYPE
INSULATED TYPE

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	1.95	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/6 module)	—	—	3.00	°C/W
R _{th(c-f)F}	Contact thermal resistance	Case to fin (per 1 module) thermal grease applied	—	—	0.067	°C/W

Note 3 : Grease with good thermal conductivity should be applied evenly with a thickness of about +100μm~+200μm on the contact surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V V _{IN} = 5V	—	1.55	2.05	V
		I _C = 20A, T _j = 25°C I _C = 20A, T _j = 125°C	—	1.65	2.15	
V _{EC}	FWDi forward voltage	T _j = 25°C, -I _C = 20A, V _{IN} = 0V	—	1.50	2.00	V
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 20A, T _j = 125°C, V _{IN} = 0 ↔ 5V Inductive load (upper-lower arm)	0.65	1.25	1.85	μs
t _{tr}			—	0.30	—	μs
t _{c(on)}			—	0.40	0.60	μs
t _{off}			—	1.50	2.10	μs
t _{c(off)}			—	0.50	0.80	μs
I _{CES}			Collector-emitter cut-off current	V _{CE} = V _{CES}	—	—
		T _j = 25°C T _j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit current	V _D = V _{DB} = 15V V _{IN} = 5V	Total of VP1-VPC, VN1-VNC	—	—	7.00	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.55	mA
		V _D = V _{DB} = 15V V _{IN} = 0V	Total of VP1-VPC, VN1-VNC	—	—	7.00	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.55	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, FO circuit pull-up to 5V with 10kΩ	4.9	—	—	V	
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA	—	—	0.95	V	
V _{SC(ref)}	Short circuit trip level	T _C = -20~100°C, V _D = 15V (Note 4)	0.45	—	0.52	V	
I _{IN}	Input current	V _{IN} = 5V	1.0	1.5	2.0	mA	
UVDBt	Control supply under-voltage protection	T _j ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width	C _{FO} = 22nF (Note 5)	1.0	1.8	—	ms	
V _{th(on)}	ON threshold voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	2.1	2.3	2.6	V	
V _{th(off)}	OFF threshold voltage		0.8	1.4	2.1	V	

Note 4 : Short circuit protection is functioning only at the low-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the collector current rating (20A).

5 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : C_{FO} = 12.2 × 10⁻⁶ × t_{FO} [F].

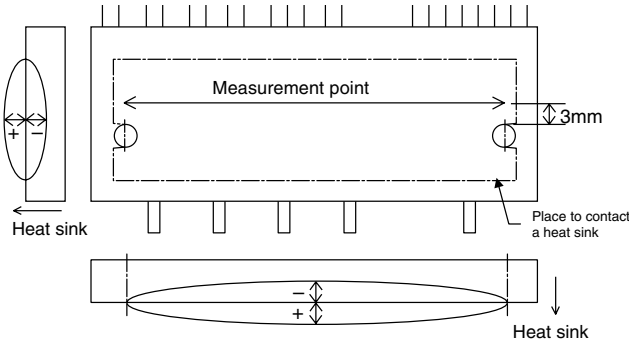
PS21265-P/AP

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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended : 1.18 N·m	0.98	—	1.47	N·m
Weight			—	54	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

Note 6 :



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Recommended value			Unit	
			Min.	Typ.	Max.		
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V	
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	13.5	15.0	16.5	V	
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.0	15.0	18.5	V	
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs	
t _{dead}	Arm shoot-through blocking time	For each input signal, T _c ≤ 100°C	2	—	—	μs	
f _{PWM}	PWM input frequency	T _c ≤ 100°C, T _j ≤ 125°C	—	—	20	kHz	
I _o	Allowable r.m.s. current	V _{CC} = 300V, V _D = V _{DB} = 15V, P.F = 0.8, sinusoidal PWM T _c ≤ 100°C, T _j ≤ 125°C (Note 7)	f _{PWM} = 5kHz	—	—	14.0	Arms
		f _{PWM} = 15kHz	—	—	9.5		
P _{WIN(on)}	Minimum input pulse width	(Note 8)		0.3	—	—	μs
P _{WIN(off)}		200 ≤ V _{CC} ≤ 350V, 13.5 ≤ V _D ≤ 16.5V, 13.0 ≤ V _{DB} ≤ 18.5V, -20°C ≤ T _c ≤ 100°C, N-line wiring inductance less than 10nH (Note 9)	Below rated current	1.4	—	—	
		Between rated current and 1.7 times of rated current	2.5	—	—		
	Between 1.7 times and 2.0 times of rated current	3.0	—	—			
V _{NC}	V _{NC} variation	between V _{NC} -N (including surge)	-5.0	—	5.0	V	

Note 7 : The Allowable r.m.s. current value depends on the actual application conditions.

8 : Input signal with ON pulse width less than P_{WIN(on)} might make no response.

9 : IPM might make no response or response delay to next turn-on pulse if off-pulse width is less than P_{WIN(off)}. (Please refer to Fig. 4) Please refer to Fig. 9 for recommended wiring method too.

PS21265-P/AP

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Fig. 4 CURRENT OUTPUT WHEN INPUT SIGNAL IS LESS THAN ALLOWABLE MINIMUM INPUT PULSE WIDTH PWIN(off) (P-side only)

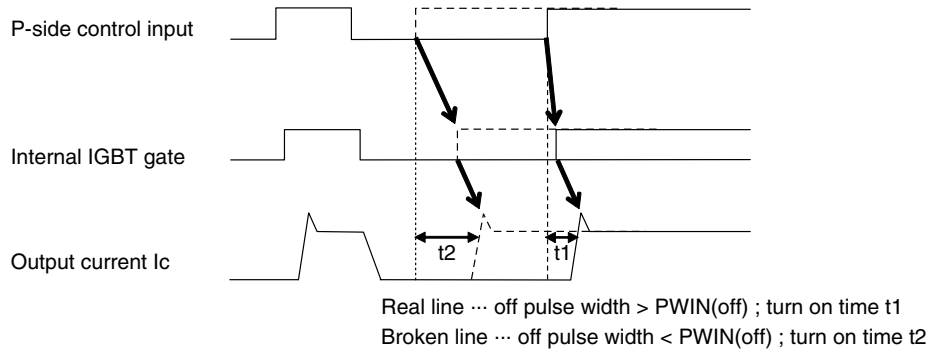
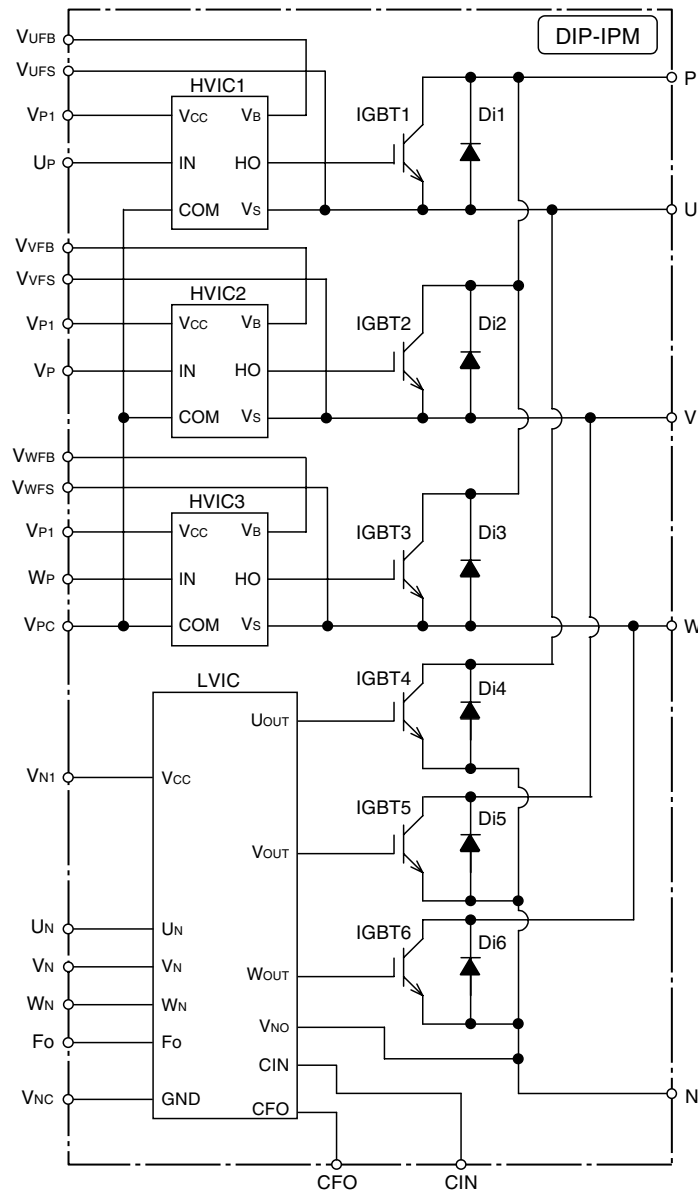


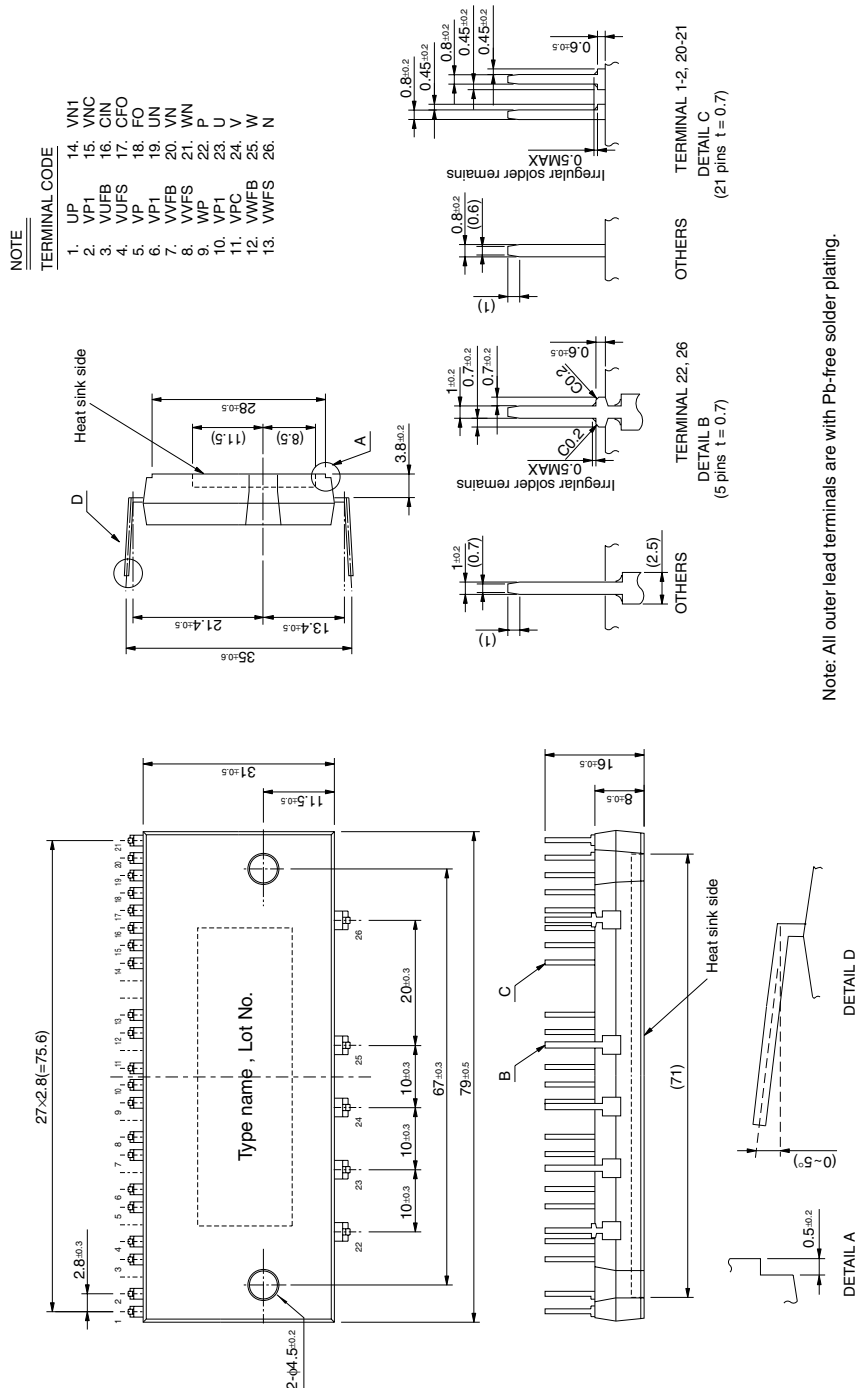
Fig. 5 THE DIP-IPM INTERNAL CIRCUIT



PS21265-P/AP

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Fig. 6 PACKAGE OUTLINES (Long-pin type : PS21265-AP)

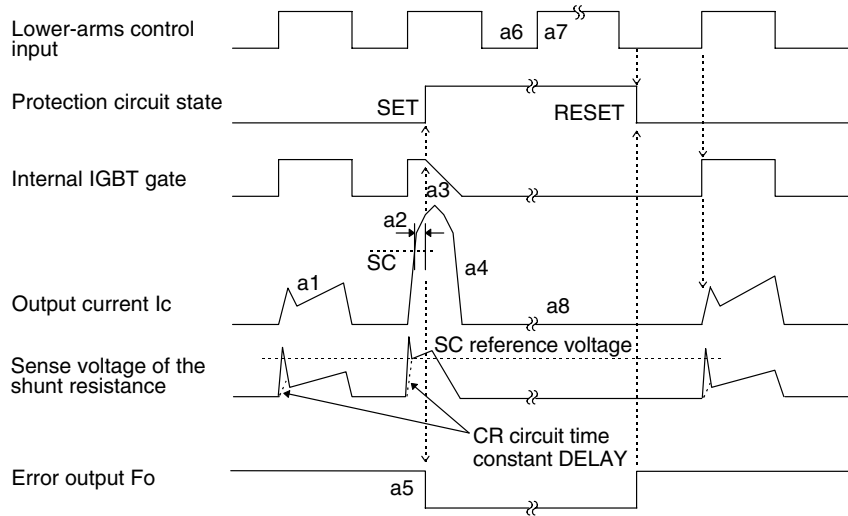


Note: All outer lead terminals are with Pb-free solder plating.

Fig. 7 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

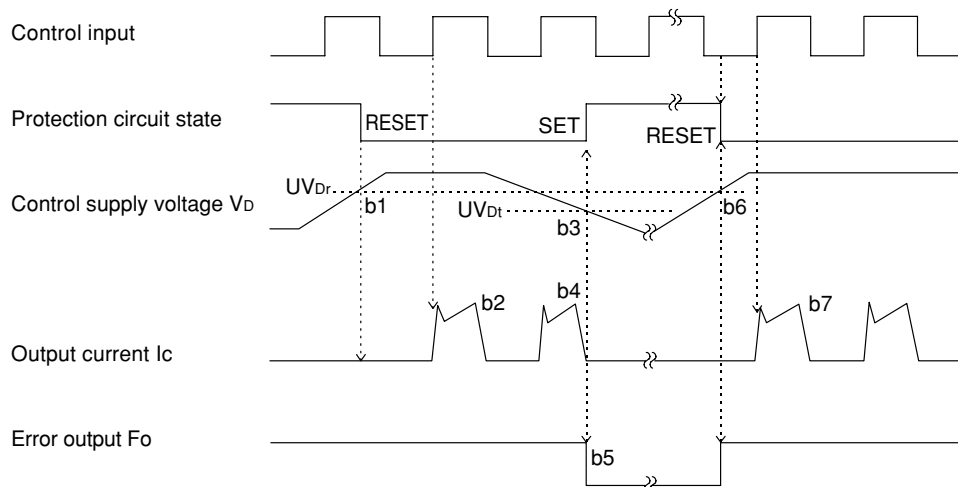
[A] Short-Circuit Protection (Lower-arms only) (with external shunt resistor and CR connection)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. Hard IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "L" : IGBT OFF state.
- a7. Input "H" : IGBT ON state, but during the Fo signal active period the IGBT doesn't turn ON.
- a8. IGBT OFF in spite of "H" input.



[B] Under-Voltage Protection (Lower-arm, UVd)

- b1. Control supply voltage rises : After the voltage reaches UV_{Dr} level, the circuits start to operate when the next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo operation starts. The minimum pulse width of Fo is set by the external capacitor C_{FO}, and Fo outputs continuously during UV period.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



PS21265-P/AP

TRANSFER-MOLD TYPE
INSULATED TYPE

[C] Under-Voltage Protection (Upper-arm, UVDB)

- c1. Control supply voltage rises : Operation starts soon after UVDBr.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

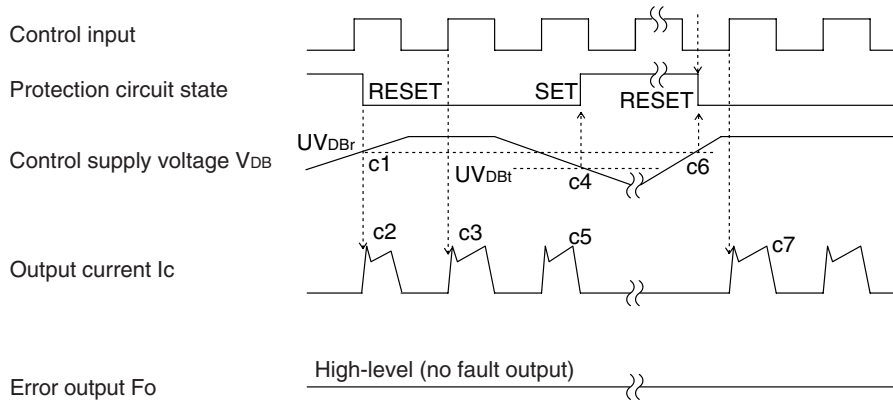
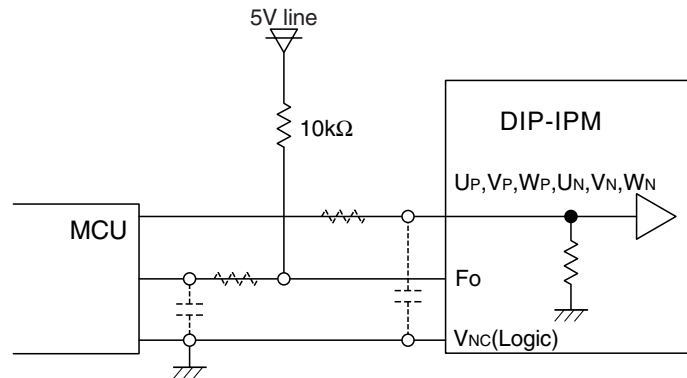
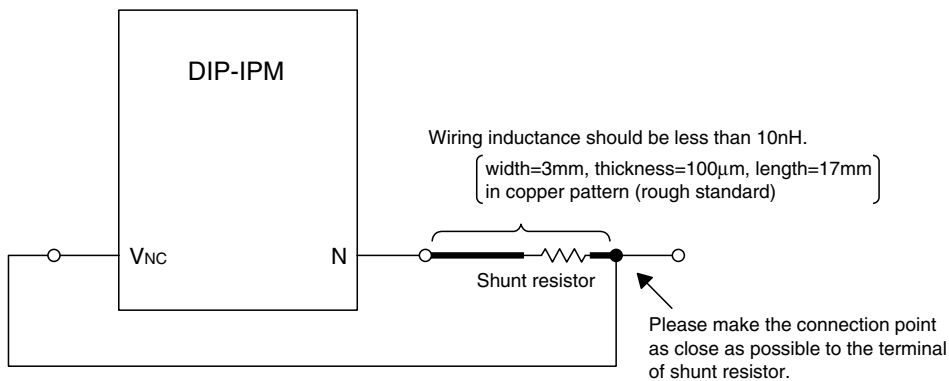


Fig. 8 RECOMMENDED MCU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, if using external RC filter, pay attention to satisfy the turn-on/off threshold voltage requirement.

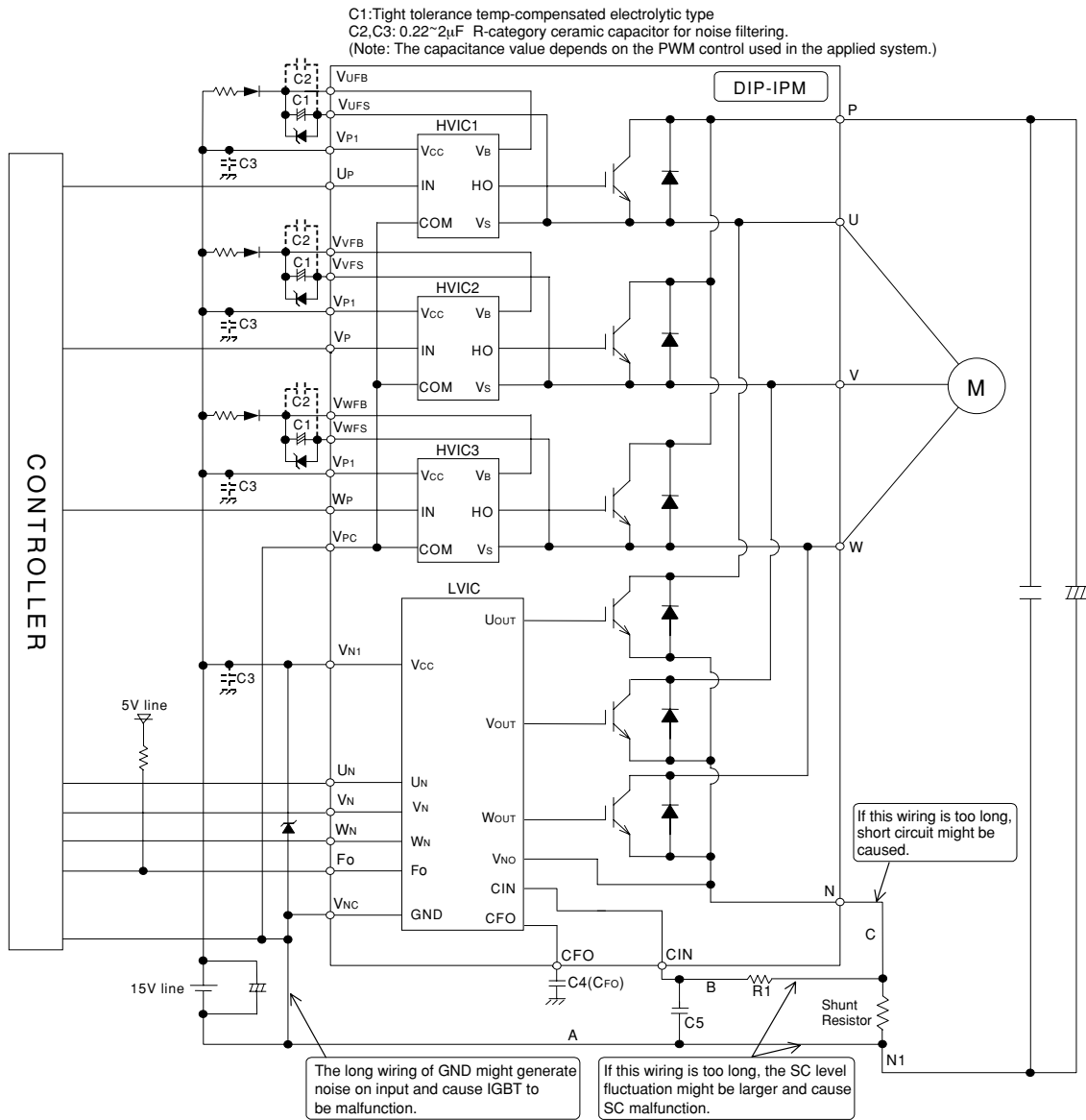
Fig. 9 RECOMMENDED WIRING OF SHUNT RESISTOR



PS21265-P/AP

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Fig. 10 EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT



- Note 1:** To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2-3cm)
- 2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3:** Fo output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.
- 4:** Fo output pulse width is determined by the external capacitor between CFO and VNC terminals (CFO). (Example : CFO = 22nF → tFO = 1.8ms (typ.))
- 5:** The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. If using external RC filter, pay attention to satisfy the turn-on/off threshold voltage requirement.
- 6:** To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.
- 7:** Please set the R1C5 time constant in the range 1.5~2μs.
- 8:** Each capacitor should be located as nearby the pins of the DIP-IPM as possible.
- 9:** To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P-N1 pins is recommended.
- 10:** To prevent ICs from surge destruction, it is recommended to insert a Zener diode (24V, 1W) between each control supply terminals.