

PM50B6LB060

FLAT-BASE TYPE
INSULATED PACKAGE

PM50B6LB060



FEATURE

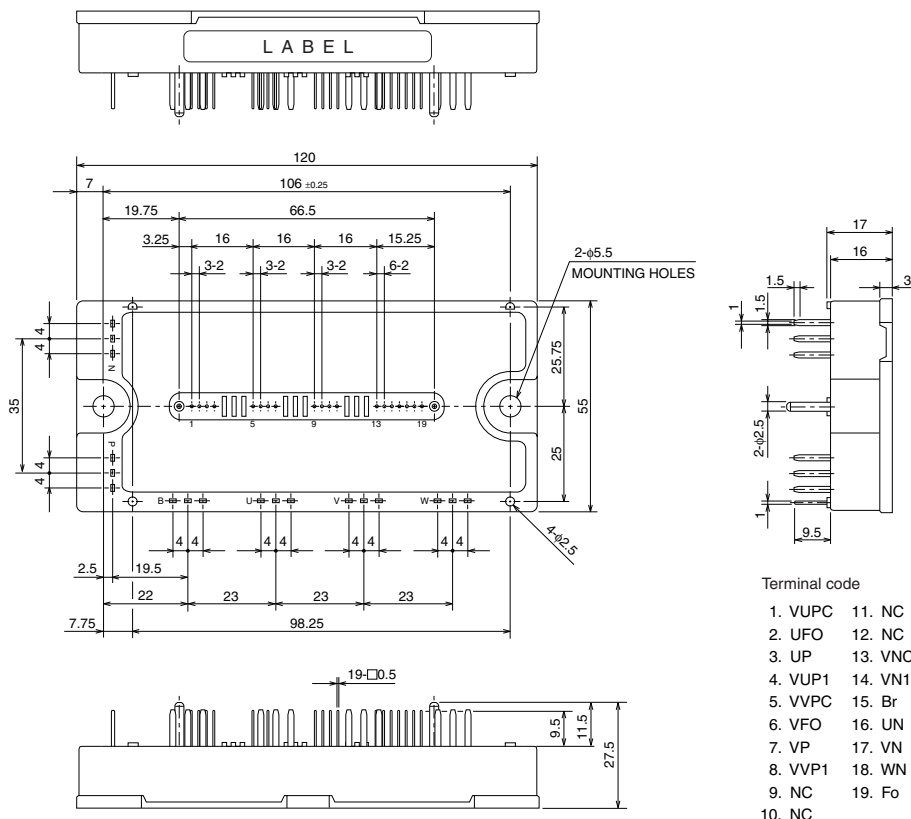
- a) Adopting new 5th generation IGBT (CSTBT™) chip, which performance is improved by 1μm fine rule process.
For example, typical $V_{ce(sat)}=1.55V @T_j=125^{\circ}C$
- b) Over-temperature protection by detecting T_j of the CSTBT™ chips and error output is possible from all each conservation upper and lower arm of IPM.
- c) New small package
Reduce the package size by 10%, thickness by 22% from S-DASH series.
 - 2φ 50A, 600V Current-sense IGBT type inverter
 - 50A, 600V Current-sense Chopper IGBT
 - Monolithic gate drive & protection logic
 - Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
 - UL Recognized Yellow Card No.E80276(N)
File No.E80271

APPLICATION

Photo voltaic power conditioner

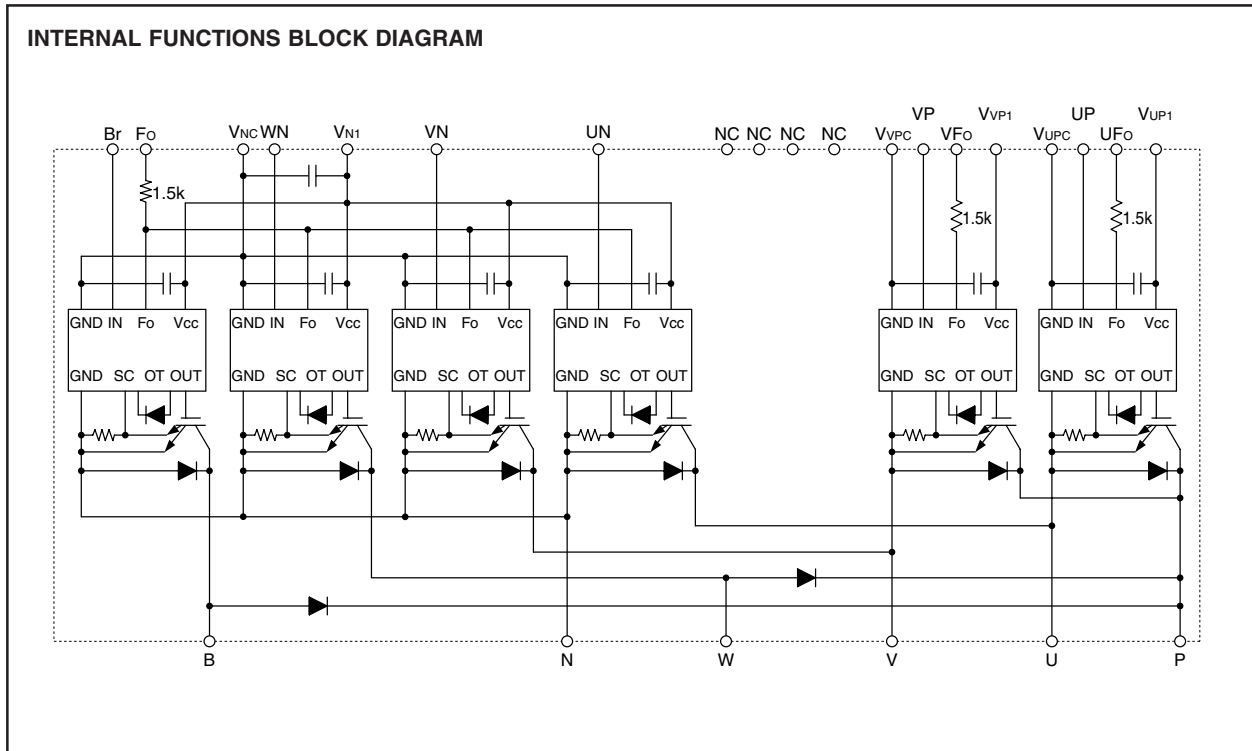
PACKAGE OUTLINES

Dimensions in mm



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$	600	V
$\pm I_C$	Collector Current	$T_c = 25^\circ\text{C}$	50	A
$\pm I_{CP}$	Collector Current (Peak)	$T_c = 25^\circ\text{C}$	100	A
P_C	Collector Dissipation	$T_c = 25^\circ\text{C}$	134	W
T_j	Junction Temperature		$-20 \sim +150$	$^\circ\text{C}$

CONVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$	600	V
I_C	Collector Current	$T_c = 25^\circ\text{C}$	50	A
I_{CP}	Collector Current (Peak)	$T_c = 25^\circ\text{C}$	100	A
P_C	Collector Dissipation	$T_c = 25^\circ\text{C}$ (Note-1)	134	W
I_F	FWDi Forward Current	$T_c = 25^\circ\text{C}$	50	A
$V_{R(DC)}$	FWDi Rated DC Reverse Voltage	$T_c = 25^\circ\text{C}$	600	V
T_j	Junction Temperature		$-20 \sim +150$	$^\circ\text{C}$

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Supply Voltage	Applied between : $V_{UP1}-V_{UPC}$ $V_{VP1}-V_{VPC}$, $V_{N1}-V_{NC}$	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC} , V_P-V_{VPC} $U_N \cdot V_N \cdot W_N \cdot B_r-V_{NC}$	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : $U_{FO}-V_{UPC}$, $V_{FO}-V_{VPC}$, $FO-V_{NC}$	20	V
I_{FO}	Fault Output Current	Sink current at U_{FO} , V_{FO} , FO terminals	20	mA

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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = +125°C Start	450	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

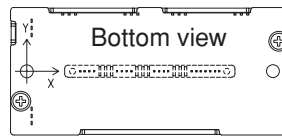
THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1/4 module) (Note-1)	—	—	0.93	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/4 module) (Note-1)	—	—	1.57	
R _{th(j-c)Q}		Converter IGBT part (Note-1)	—	—	0.93	
R _{th(j-c)F}		Converter FWDi upper part (Note-1)	—	—	0.96	
R _{th(j-c)F}		Converter FWDi lower part (Note-1)	—	—	1.57	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.038	

(Note-1) T_c (under the chip) measurement point is below.

(unit : mm)

axis \ arm	UP		VP		WP	BP	UN		VN		WN		BN	
	IGBT	FWDi	IGBT	FWDi	FWDi	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	32.7	32.2	64.6	66.1	83.6	24.6	39.8	40.3	56.5	56.0	75.5	75.0	19.1	25.9
Y	-6.4	0.4	-7.8	-1.0	-4.8	5.8	7.2	0.4	2.8	-4.0	2.8	-4.0	-8.4	-9.0



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CIN} = 0V (Fig. 1)	T _j = 25°C	—	1.7	2.3	V
			T _j = 125°C	—	1.55	2.0	
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _D = 15V, V _{CIN} = 15V (Fig. 2)	—	2.2	3.3	V	
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V ↔ 15V V _{CC} = 300V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4)	—	0.3	0.7	1.4	μs
t _{tr}			—	0.1	0.2		
t _{c(on)}			—	0.2	0.4		
t _{off}			—	0.9	1.8		
t _{c(off)}			—	0.2	0.4		
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 5)	T _j = 25°C	—	—	1	mA
			T _j = 125°C	—	—	10	

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Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CIN} = 0V, Pulsed (Fig. 1)	T _J = 25°C	—	1.7	2.3	V
			T _J = 125°C	—	1.55	2.0	
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _{CIN} = 15V, V _D = 15V (Fig. 2)	—	2.2	3.3	V	
V _{FM}	Forward Voltage	I _F = 50A	—	1.9	3.0	V	
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 300V, I _C = 50A T _J = 125°C Inductive Load (Fig. 3,4)	—	0.3	0.7	1.4	μs
t _{tr}			—	—	0.1	0.2	
t _{c(on)}			—	—	0.2	0.4	
t _{off}			—	—	0.9	1.8	
t _{c(off)}			—	—	0.2	0.4	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 5)	T _J = 25°C	—	—	1	mA
			T _J = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit Current	V _D = 15V, V _{CIN} = 15V	V _{N1} -V _{Nc}	—	20	30	mA
			V*P1-V*PC	—	5	10	
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC UN • VN • WN • Br-VNC	—	1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Threshold Voltage		—	1.7	2.0	2.3	
SC	Short Circuit Trip Level	-20 ≤ T _J ≤ 125°C, V _D = 15V (Fig. 3,6)	Inverter part	100	—	—	A
			Converter part	100	—	—	
t _{off(SC)}	Short Circuit Current Delay Time	V _D = 15V (Fig. 3,6)	—	0.2	—	μs	
OT	Over Temperature Protection	V _D = 15V Detect T _J of IGBT chip	Trip level	135	145	—	°C
			Reset level	—	125	—	
UV	Supply Circuit Under-Voltage Protection	-20 ≤ T _J ≤ 125°C	Trip level	11.5	12.0	12.5	V
			Reset level	—	12.5	—	
I _{FO(H)}	Fault Output Current	V _D = 15V, V _{FO} = 15V (Note-2)	—	—	0.01	mA	
I _{FO(L)}			—	10	15		
t _{FO}	Minimum Fault Output Pulse Width	V _D = 15V (Note-2)	1.0	1.8	—	ms	

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	340	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 450	V
V _D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC V _{N1} -V _{Nc} (Note-3)	15 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC UN • VN • WN • Br-VNC	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 9.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t _{dead}	Arm Short-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.0	μs

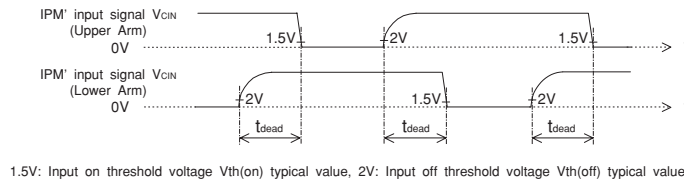
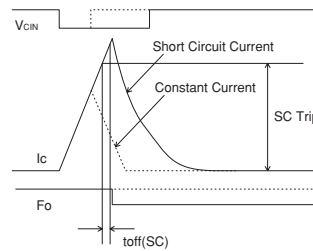
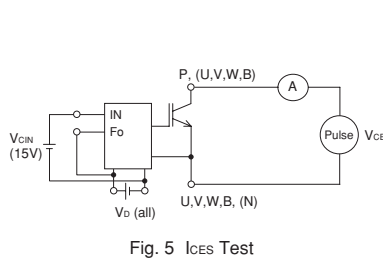
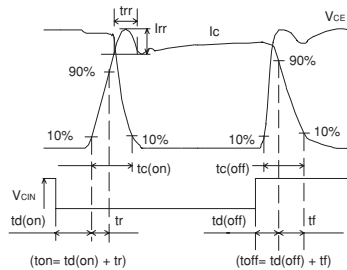
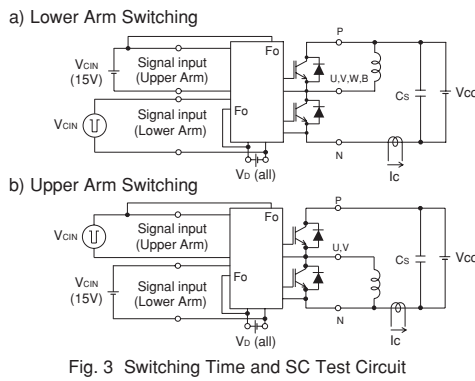
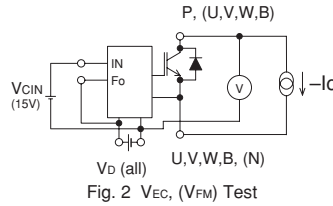
(Note-3) With ripple satisfying the following conditions : dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

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PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)



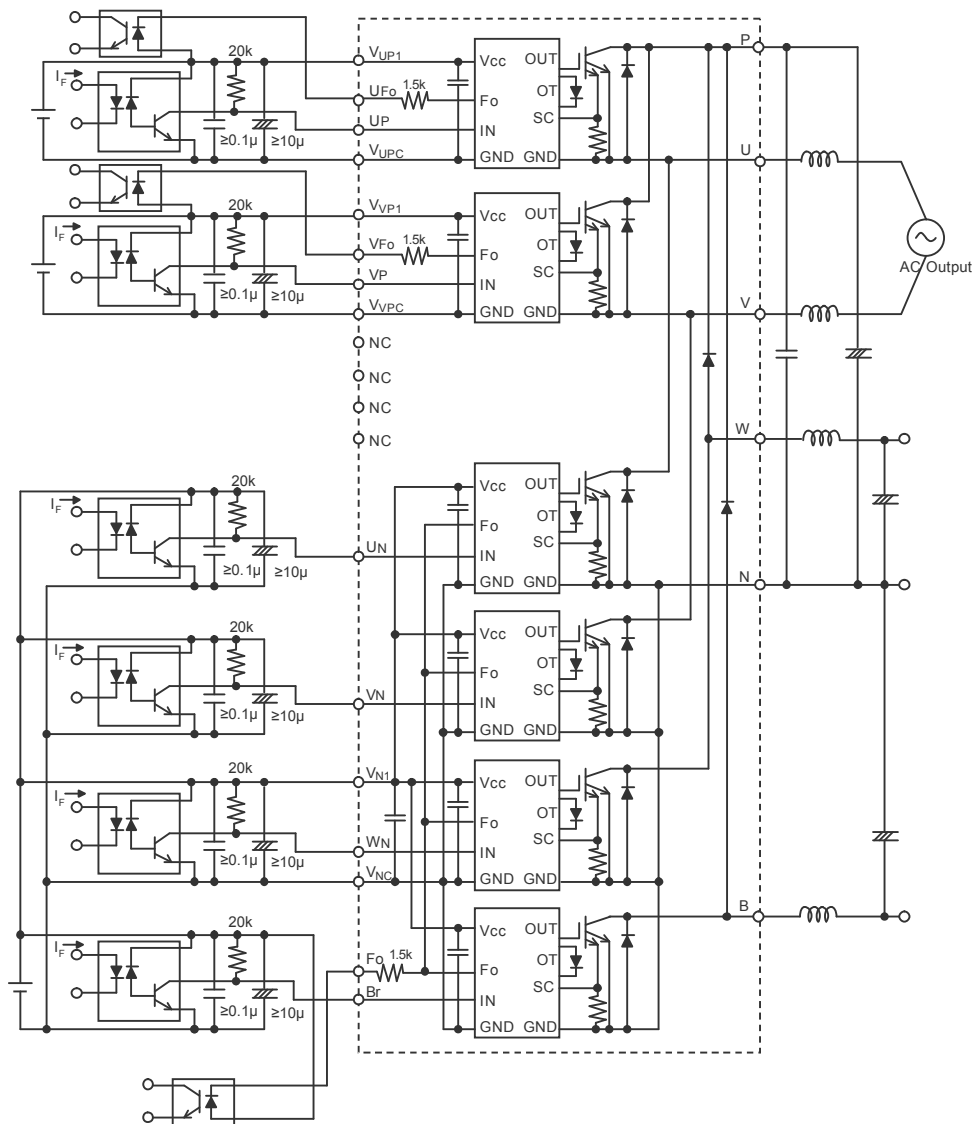


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

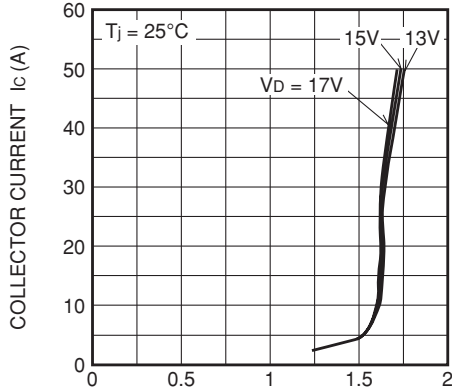
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-coupler: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 3 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

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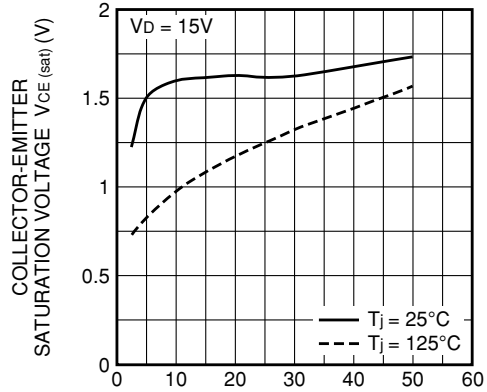
PERFORMANCE CURVES (INVERTER PART)

OUTPUT CHARACTERISTICS (TYPICAL)



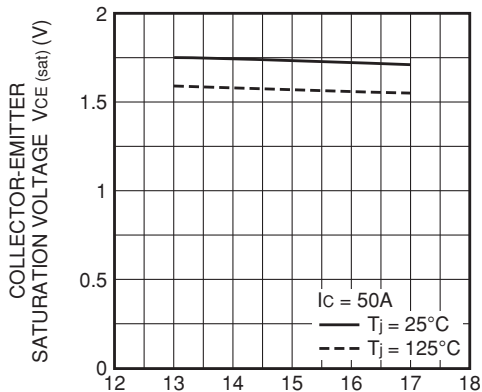
COLLECTOR-EMITTER SATURATION VOLTAGE $V_{ce(sat)}$ (V)

COLLECTOR-EMITTER SATURATION VOLTAGE (VS. I_c) CHARACTERISTICS (TYPICAL)



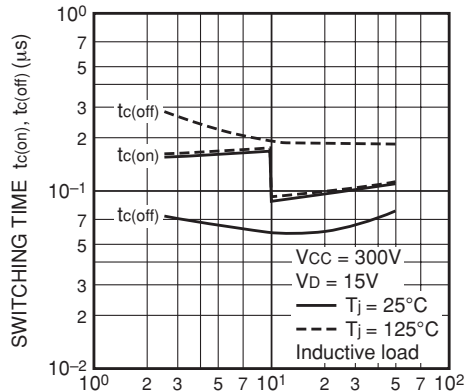
COLLECTOR CURRENT I_c (A)

COLLECTOR-EMITTER SATURATION VOLTAGE (VS. V_D) CHARACTERISTICS (TYPICAL)



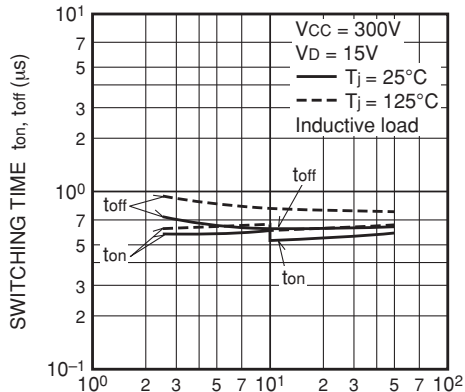
CONTROL SUPPLY VOLTAGE V_D (V)

SWITCHING TIME CHARACTERISTICS (TYPICAL)



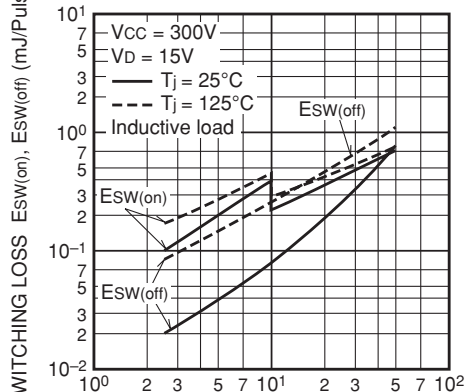
COLLECTOR CURRENT I_c (A)

SWITCHING TIME CHARACTERISTICS (TYPICAL)



COLLECTOR CURRENT I_c (A)

SWITCHING LOSS CHARACTERISTICS (TYPICAL)

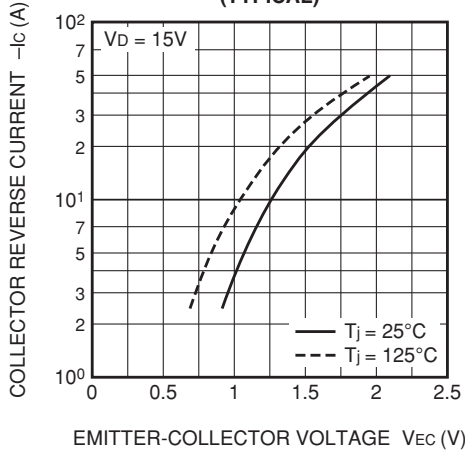


COLLECTOR CURRENT I_c (A)

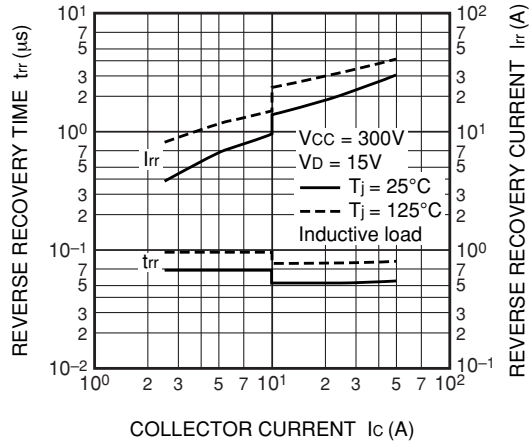
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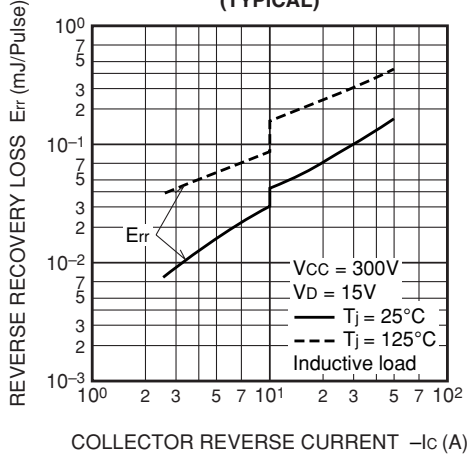
FWDi FORWARD VOLTAGE CHARACTERISTICS (TYPICAL)



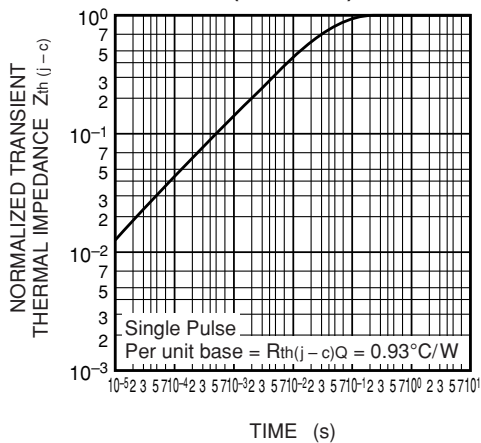
FWDi REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



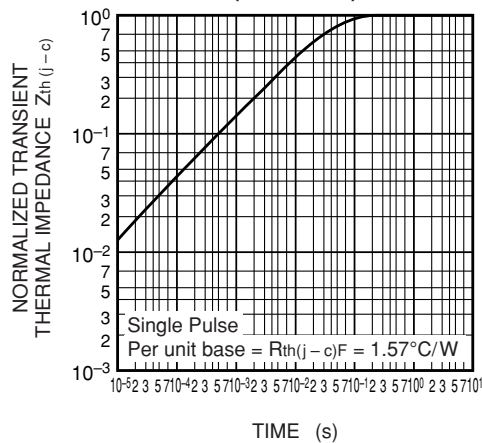
FWDi REVERSE RECOVERY LOSS CHARACTERISTICS (TYPICAL)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (IGBT PART)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (FWDi PART)

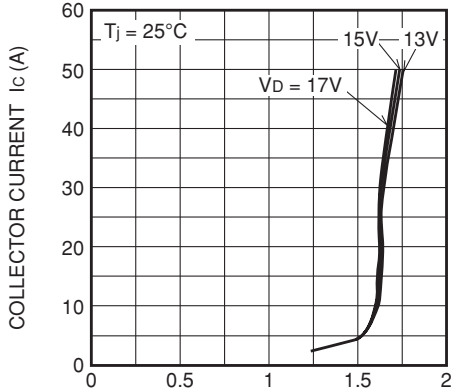


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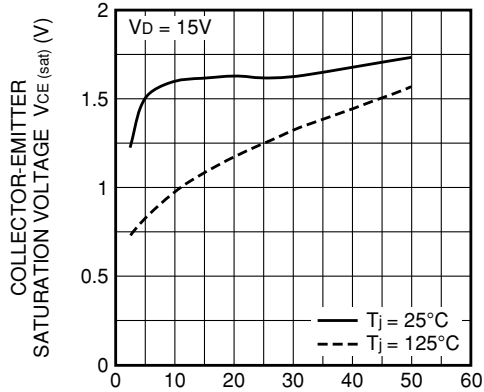
(CONVERTER PART)

OUTPUT CHARACTERISTICS (TYPICAL)



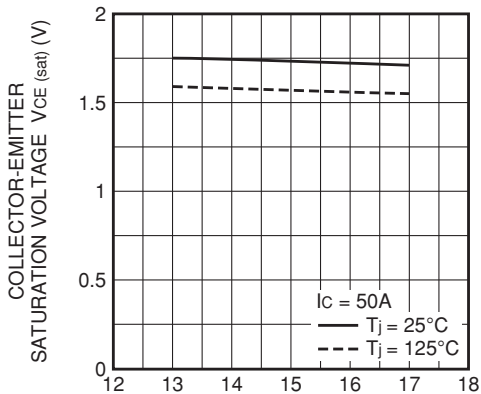
COLLECTOR-EMITTER SATURATION VOLTAGE $V_{CE(sat)}$ (V)

COLLECTOR-EMITTER SATURATION VOLTAGE (VS. I_c) CHARACTERISTICS (TYPICAL)



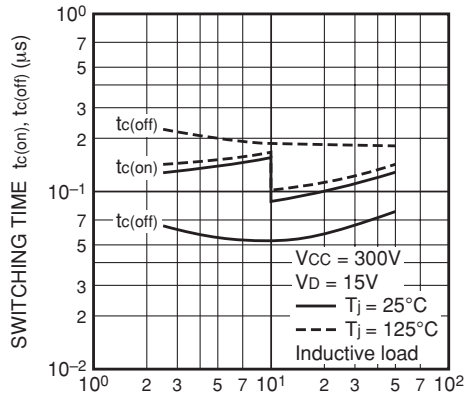
COLLECTOR CURRENT I_c (A)

COLLECTOR-EMITTER SATURATION VOLTAGE (VS. V_D) CHARACTERISTICS (TYPICAL)



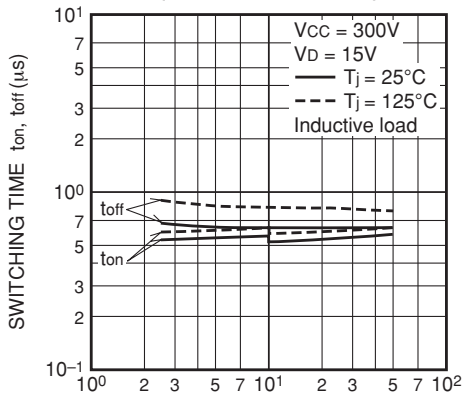
CONTROL SUPPLY VOLTAGE V_D (V)

SWITCHING TIME CHARACTERISTICS (Lower Arm - TYPICAL)



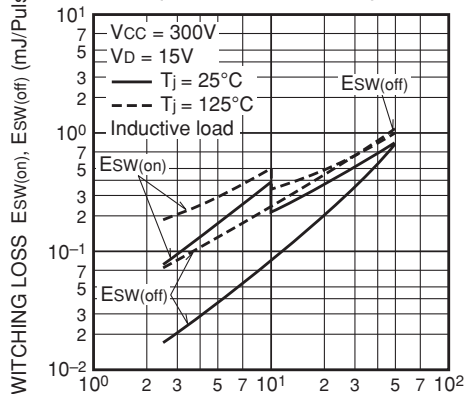
COLLECTOR CURRENT I_c (A)

SWITCHING TIME CHARACTERISTICS (Lower Arm - TYPICAL)



COLLECTOR CURRENT I_c (A)

SWITCHING LOSS CHARACTERISTICS (Lower Arm - TYPICAL)

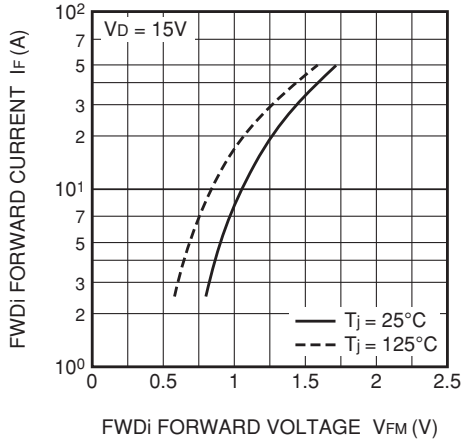


COLLECTOR CURRENT I_c (A)

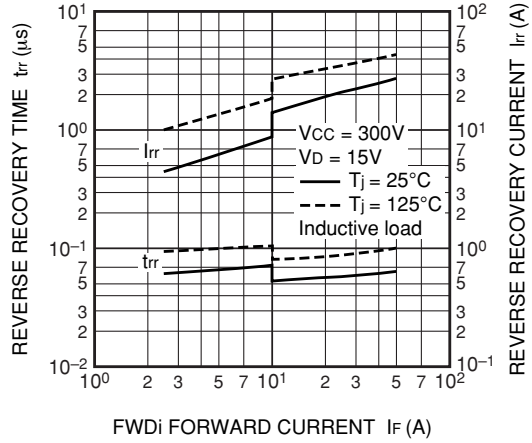
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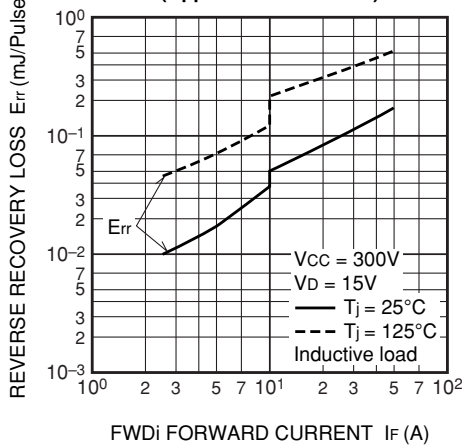
FWDi FORWARD VOLTAGE CHARACTERISTICS
(Upper Arm · TYPICAL)



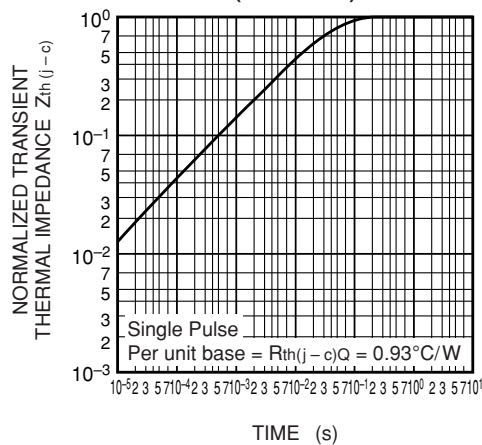
FWDi REVERSE RECOVERY CHARACTERISTICS
(Upper Arm · TYPICAL)



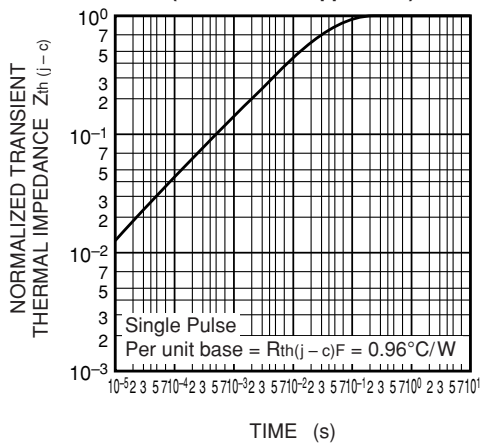
FWDi REVERSE RECOVERY LOSS CHARACTERISTICS
(Upper Arm · TYPICAL)



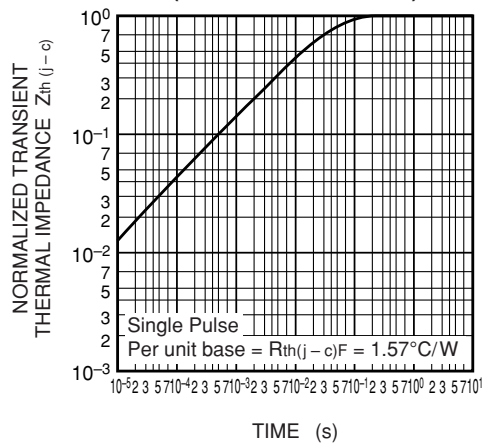
TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS
(IGBT PART)



TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS
(FWDi PART · Upper Arm)



TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS
(FWDi PART · Lower Arm)



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