MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

< HVIC >

M81740FP

HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81740FP is high voltage Power MOSFET and IGBT gate driver for half bridge applications.

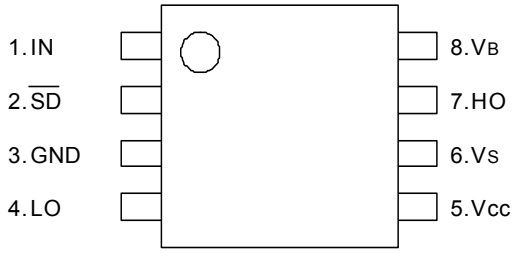
FEATURES

- Floating Supply Voltage ·····600v
- Output Current ····· ±3.25A (Typ.)
- Two Input Type ·····IN/$\overline{SD}$
- Internally Set Deadtime
- 3.3v And 5v Input Logic Compartible.
- Half Bridge Driver
- Undervoltage Lockout
- SOP-8 Package

APPLICATIONS

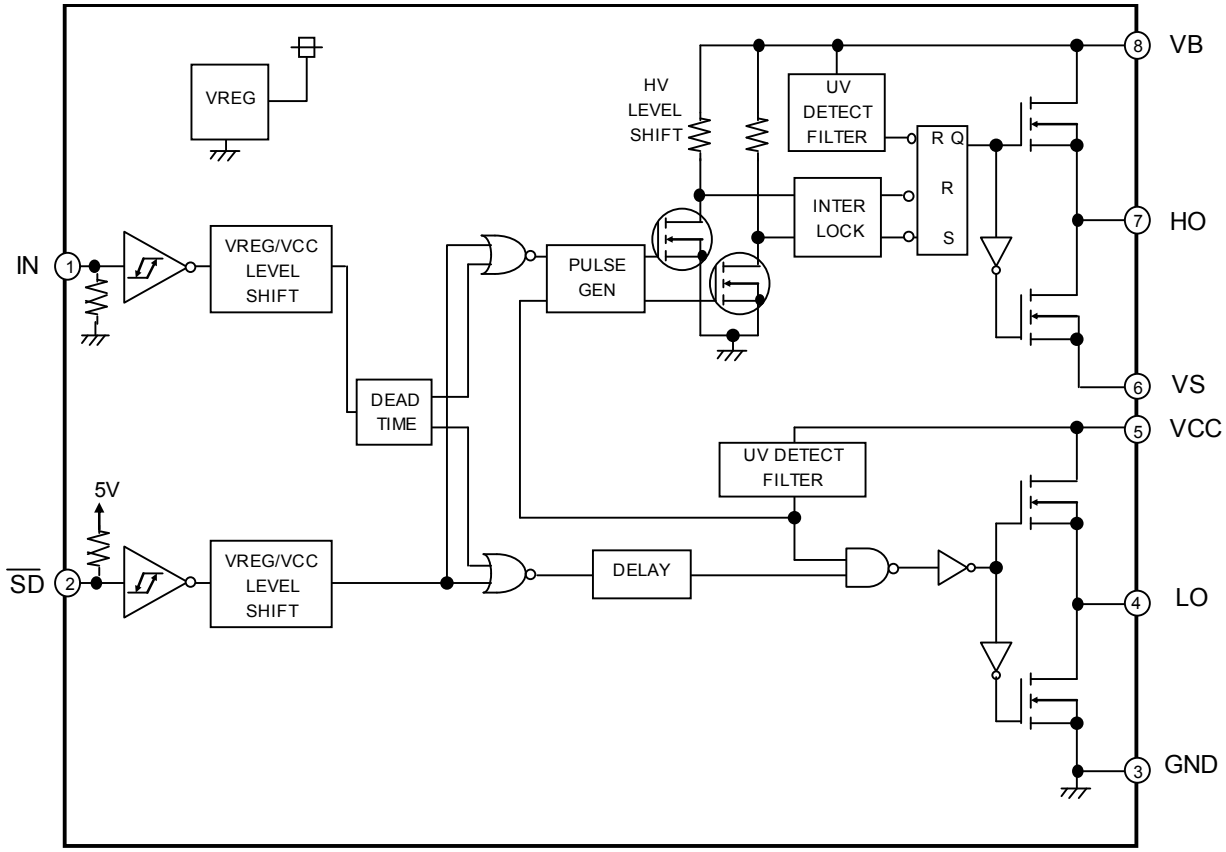
MOSFET and IGBT gate driver for Lighting, refrigerator, air-conditioner, washing machine, inverter and general purpose.

PIN CONFIGURATION (TOP VIEW)

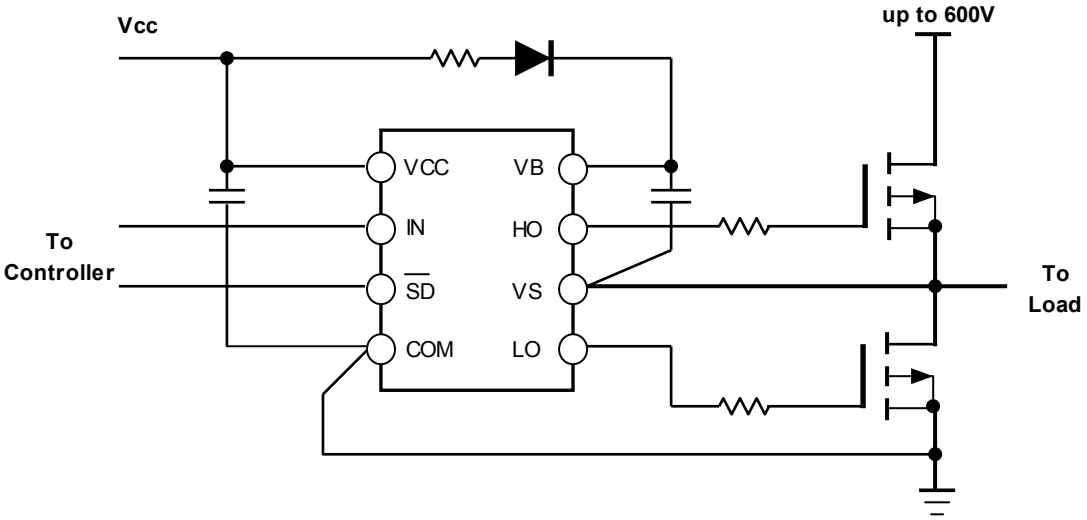


Outline:8P2S
(Pb Free)

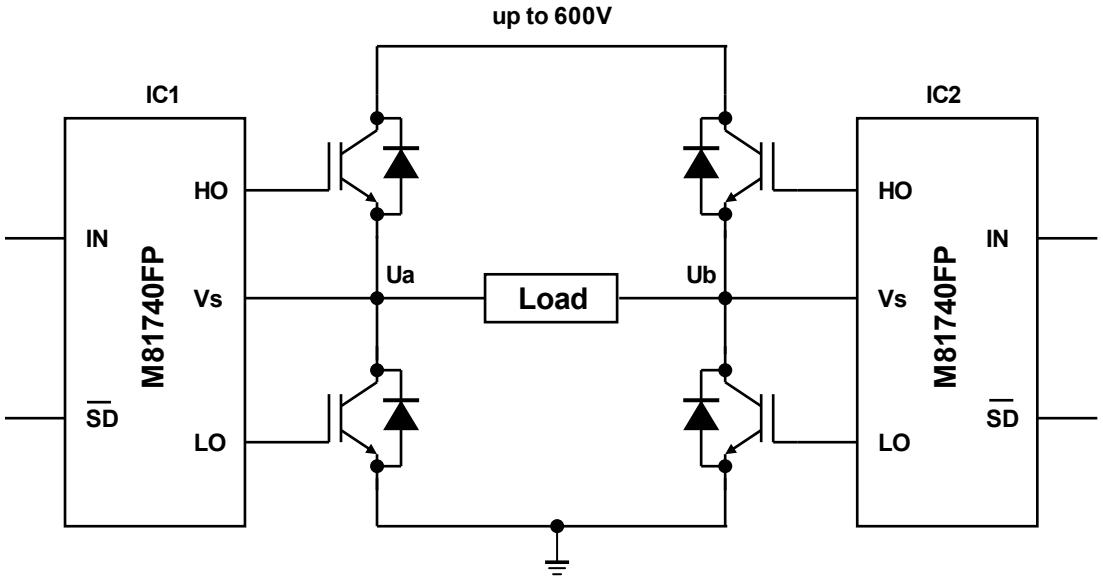
BLOCK DIAGRAM



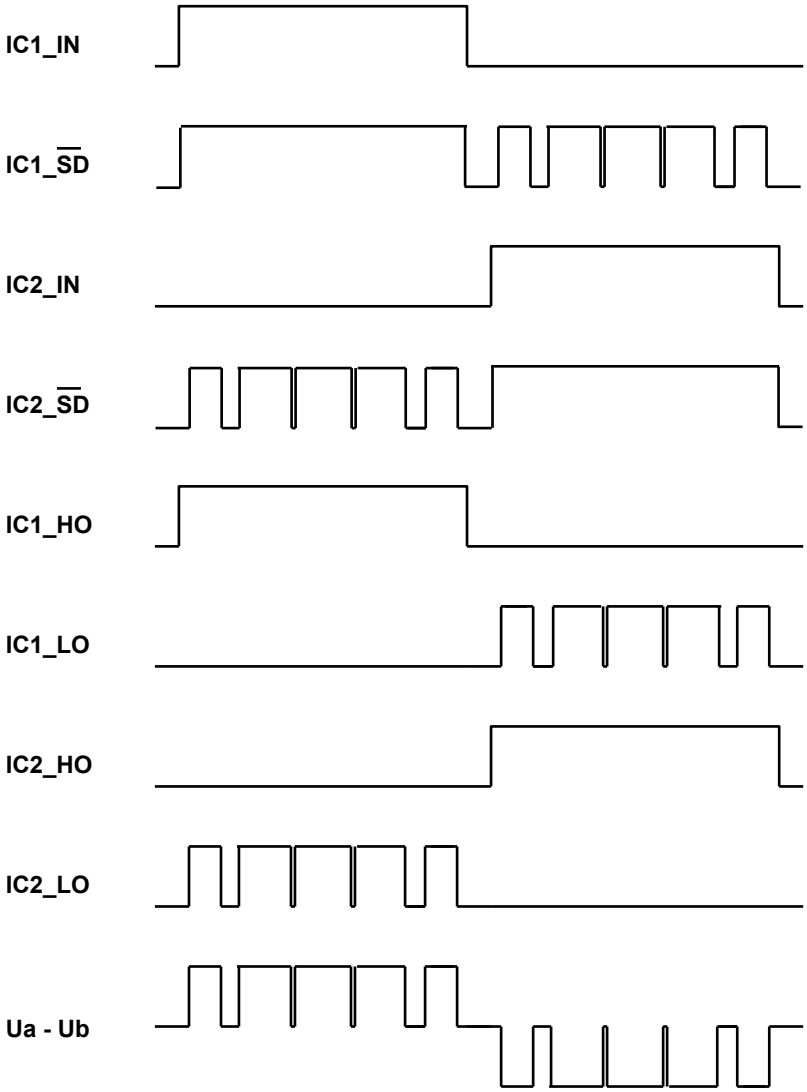
TYPICAL CONNECTION (General Purpose)



TYPICAL CONNECTION (In Unipolar Modulation PWM Application)



SEQUENCE ($\overline{SD}$ is used as low side input terminal)



ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified)

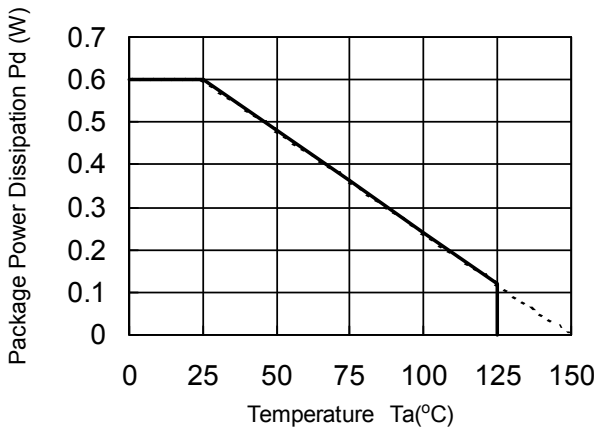
Symbol	Parameter	Test conditions	Ratings	Unit
V_B	High Side Floating Supply Absolute Voltage		-0.3 ~ 624	V
V_S	High Side Floating Supply Offset Voltage		V_B-24 ~ V_B+0.3	V
V_{BS}	High Side Floating Supply Voltage	$V_{BS}=V_B-V_S$	-0.3 ~ 24	V
V_{HO}	High Side Output Voltage		V_S-0.3 ~ V_B+0.3	V
V_{CC}	Low Side Fixed Supply Voltage		-0.3 ~ 24	V
V_{LO}	Low Side Output Voltage		-0.3 ~ Vcc+0.3	V
V_{IN}	Logic Input Voltage (IN & $\overline{SD}$)		-0.3 ~ Vcc+0.3	V
dV_S/dt	Allowable Offset Voltage Transient		±50	V/ns
Pd	Package Power Dissipation	Ta= 25 °C ,On Board	0.6	W
Kθ	Linear Derating Factor	Ta> 25 °C ,On Board	4.8	mW/°C
Rth(j-c)	Junction-Case Thermal Resistance		50	°C/W
Tj	Junction Temperature		-40 ~ +150	℃
Topr	Operation Temperature		-40 ~ +125	℃
Tstg	Storage Temperature		-40 ~ +150	℃
TL	Solder Heatproof	RoHS Correspondence	255:10s,max 260	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_B	High Side Floating Supply Absolute Voltage		V_S+10	—	V_S+20	V
V_S	High Side Floating Supply Offset Voltage	V_B>10V	-5	—	500	V
V_{BS}	High Side Floating Supply Voltage	$V_{BS}=V_B-V_S$	10	—	20	V
V_{HO}	High Side Output Voltage		V_S	—	V_B	V
V_{CC}	Low Side Fixed Supply Voltage		10	—	20	V
V_{LO}	Low Side Output Voltage		0	—	V_{CC}	V
V_{IN}	Logic Input Voltage (IN & $\overline{SD}$)		0	—	5	V

* For proper operation, the device should be used within the recommended conditions

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)

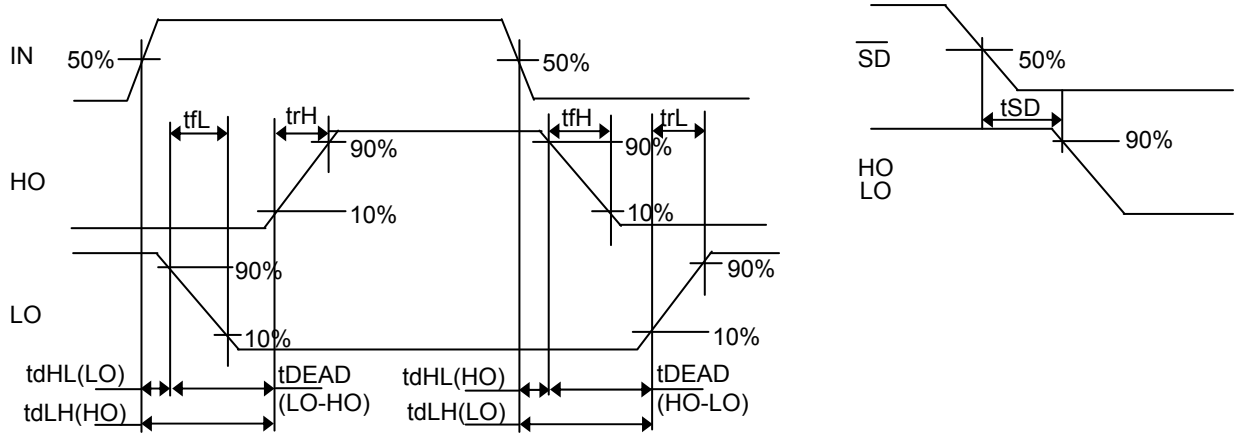


ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=V_{BS}(=V_B-V_S)=15V, unless otherwise specified)

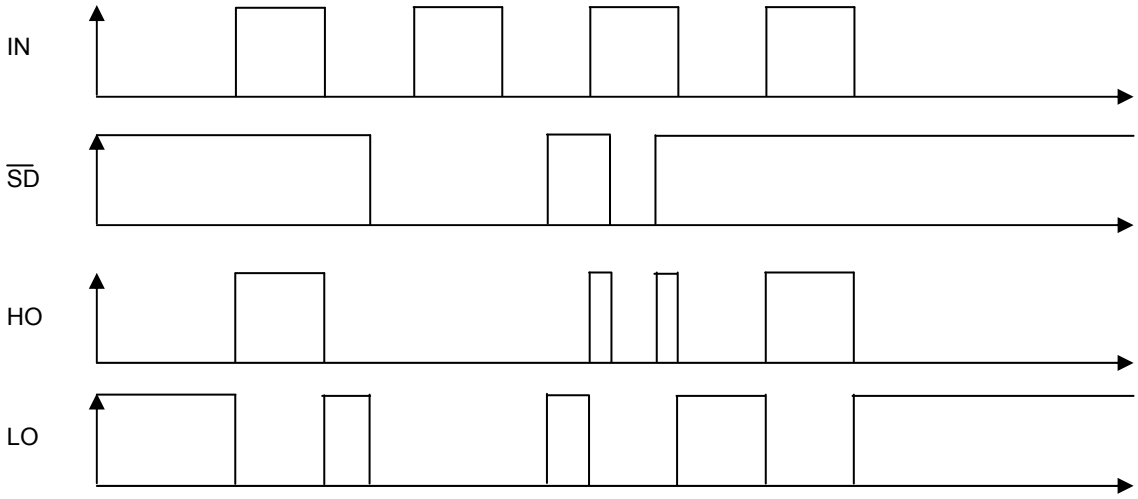
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
I_{FS}	Floating Supply Leakage Current	V_B = V_S = 600V	—	—	1.0	μA
I_{BS}	V_{BS} Standby Current	IN = 0V or 5V	—	0.2	0.5	mA
I_{CC}	V_{CC} Standby Current	IN = 0V or 5V	0.2	0.6	1.0	mA
V_{OH}	High Level Output Voltage	I_O = 0mA, LO, HO	13.8	14.4	—	V
V_{OL}	Low Level Output Voltage	I_O = 20mA, LO, HO	—	—	0.2	V
V_{IH}(IN)	High Level Input Threshold Voltage (V_{IN})		—	2.2	2.7	V
V_{IL}(IN)	Low Level Input Threshold Voltage (V_{IN})		0.8	1.6	—	V
V_{IH}(SD)	High Level Input Threshold Voltage ($V_{\overline{SD}}$)		—	2.2	2.7	V
V_{IL}(SD)	Low Level Input Threshold Voltage ($V_{\overline{SD}}$)		0.8	1.6	—	V
I_{IH}	High Level Input Bias Current	V_{IN} = 5V ,$V_{\overline{SD}}$=0V	—	25	60	μA
I_{IL}	Low Level Input Bias Current	V_{IN} = 0V ,$V_{\overline{SD}}$=5V	—	—	5	μA
V_{BSuvr}	V_{BS} Supply UV Reset Voltage		7.0	8.4	9.8	V
V_{BSuvh}	V_{BS} Supply UV Hysteresis Voltage		0.3	0.5	—	V
t_{VBSuv}	V_{BS} Supply UV Filter Time		—	7.5	—	μs
V_{CCuvr}	V_{CC} Supply UV Reset Voltage		7.0	8.4	9.8	V
V_{CCuvh}	V_{CC} Supply UV Hysteresis Voltage		0.3	0.5	—	V
t_{VCCuv}	V_{CC} Supply UV Filter Time		—	7.5	—	μs
I_{OH}	Output High Level Short Circuit Pulsed Current	V_O = 0V, PW < 10μs	2.3	3.25	—	A
I_{OL}	Output Low Level Short Circuit Pulsed Current	V_O = 15V, PW < 10μs	2.3	3.25	—	A
t_{dLH}	Turn-On Propagation Delay	CL = 1000pF between HO-V_S, LO-GND V_{IN} = 0 ~ 5V	—	—	900	ns
t_{dHL}	Turn-Off Propagation Delay	CL = 1000pF between HO-V_S , LO-GND V_{IN} = 0 ~ 5V	—	—	400	ns
tSD	Shut Down Propagation Delay		—	—	270	ns
⊿tdLH	Turn-On Propagation Delay Matching	|tdLH(HO)-tdLH(LO)|	—	0	90	ns
⊿tdHL	Turn-Off Propagation Delay Matching	|tdHL(HO)-tdHL(LO)|	—	0	40	ns
t_{rH}	High Side Turn-On Rise Time	CL = 1000pF between HO-V_S	—	—	60	ns
t_{fH}	High Side Turn-Off Fall Time	CL = 1000pF between HO-V_S	—	—	35	ns
t_{rL}	Low Side Turn-On Rise Time	CL = 1000pF between LO-GND	—	—	60	ns
t_{fL}	Low Side Turn-Off Fall Time	CL = 1000pF between LO-GND	—	—	35	ns
tDEAD	Dead Time LO Turn-Off to HO Turn-On & HO Turn-Off to LO Turn-On	CL = 1000pF between HO-V_S, LO-GND V_{IN} = 0 ~ 5V	—	400	—	ns
⊿tDEAD	Dead Time Matching	|tDEAD(LO-HO)-tDEAD(HO-LO)|	—	0	50	ns

* Typ. is not specified.

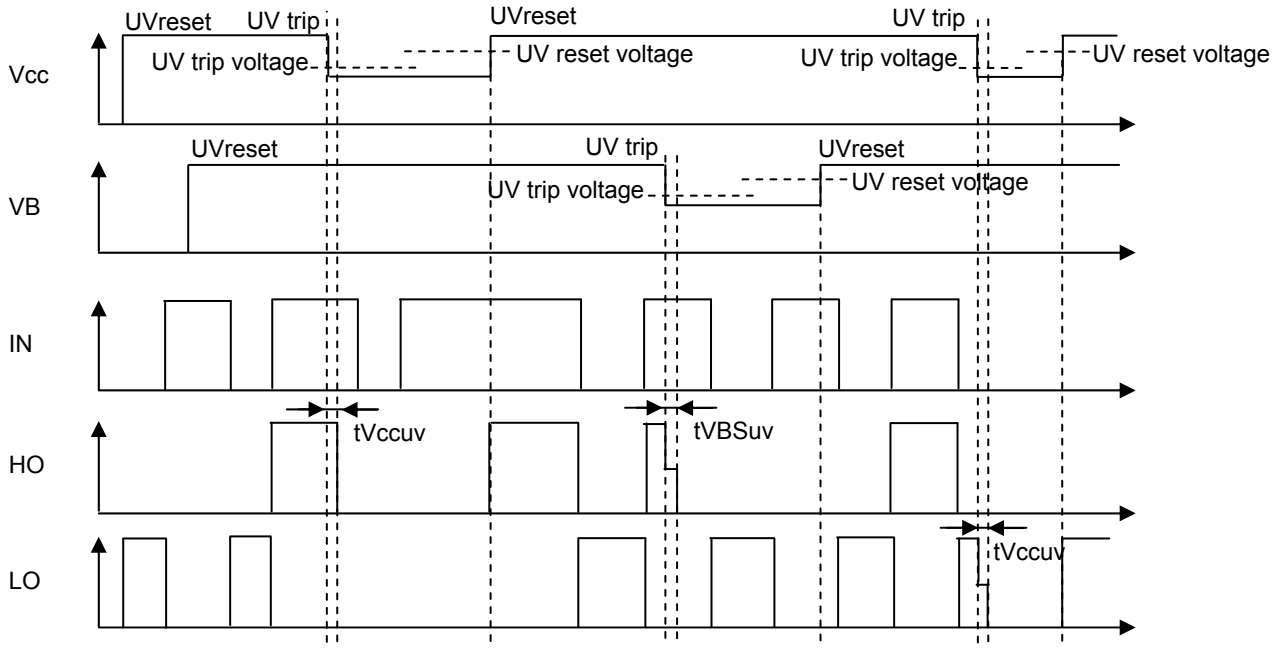
INPUT/OUTPUT TIMING DIAGRAM



FUNCTION TIMING DIAGRAM 1

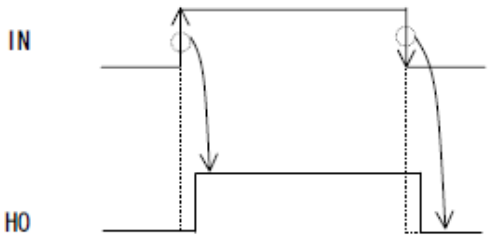


FUNCTION TIMING DIAGRAM 2



1. HO has positive logic with reference to IN. LO has negative logic with reference to IN.

2. Output signal (HO) is triggered by the edge of input signal.



3. Logic During UV(V_{CC}, V_{BS}) Error

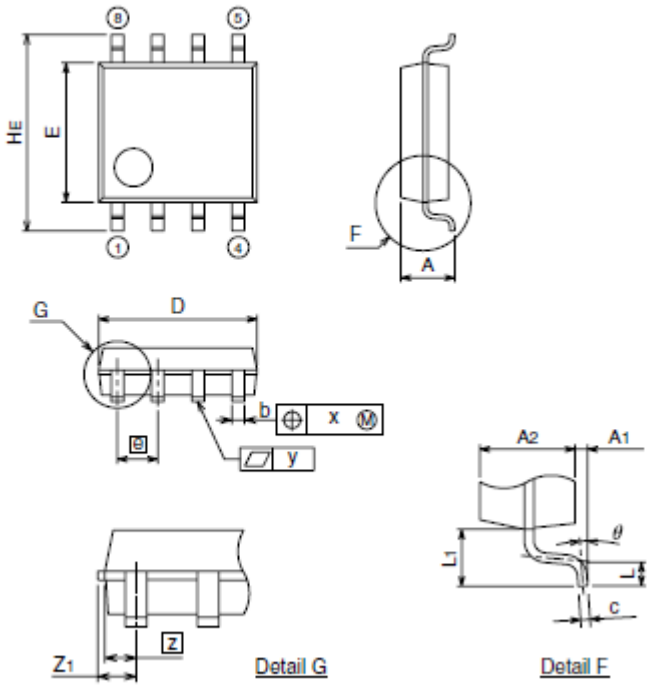
Error Signal	HO	LO
UV error (V_{CC})	HO is locked at "L" level as long as UV error for V_{CC} is detected. After V_{CC} exceeds V_{CC} UV reset level, the lock for HO is removed and responds to IN signal. (V_{CC}>V_{BS})	LO is locked at "L" level as long as UV error for V_{CC} is detected. After V_{CC} exceeds V_{CC} UV reset level, the lock for LO is removed and responds to IN signal.
UV error (V_{BS})	HO is locked at "L" level as long as UV error for V_{BS} is detected. After V_{BS} UV reset level, the lock for HO is removed following an "L" state of the IN signal, and then HO responds to the input.	LO is independent of V_{BS} to respond to IN.

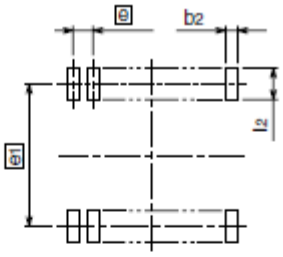
*IF UV error for V_{CC} is detected when HO is in "H" level and the falling speed of V_{CC} is exceeds 0.03V/μs, the off signal for HO might not be transmitted from low side to high side and then HO stays "H".

4. Supply start up sequence

Please start up V_{CC} supply and V_{BS} supply in that order, and, please shut down V_{BS} supply and V_{CC} supply in that order. Please start up V_{CC} supply and V_{BS} supply with gentle slope. If you start up supply with sharp slope, there is some possibility that HO or LO outputs "H" for a moment.
If V_{CC} supply is less than 10V(outside of RECOMMENDED OPERATING CONDITIONS), there is some possibility that output does not change in response to input. Please evaluate carefully about supply start up or restart after shut down in your application systems.

PACKAGE OUTLINE





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.9
A1	0.05	–	–
A2	–	1.5	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	4.8	5.0	5.2
E	4.2	4.4	4.6
θ	–	1.27	–
HE	5.9	6.2	6.5
L	0.2	0.4	0.6
L1	–	0.9	–
Z	–	0.595	–
Z1	–	–	0.745
x	–	–	0.25
y	–	–	0.1
θ	0°	–	10°
b2	–	0.76	–
θ1	–	5.72	–
l2	1.27	–	–

Main Revision for this Edition

No.	Date	Revision	
		Pages	Points
A	2012.01.26	-	New

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