

M81712FP

HIGH VOLTAGE THREE PHASE BRIDGE DRIVER

DESCRIPTION

M81712FP is high voltage Power MOSFET and IGBT module driver for THREE PHASE bridge applications.

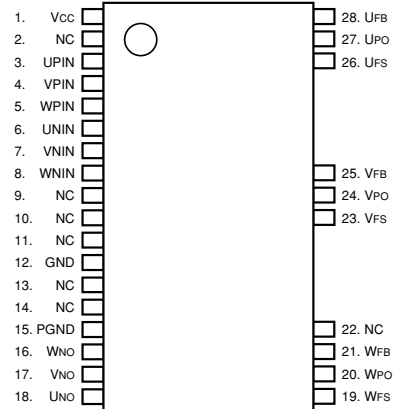
FEATURES

- FLOATING SUPPLY VOLTAGE 600V
- OUTPUT CURRENT +200mA/-500mA (typ)
- THREE PHASE BRIDGE DRIVER
- 28Pin SSOP PACKAGE (Cut Pin Package)
DISTANCE BETWEEN HIGHSIDE-PHASE : 3.4mm

APPLICATIONS

MOSFET and IGBT module inverter driver for refrigerator, air-conditioner, washing machine, AC-servomotor and general purpose.

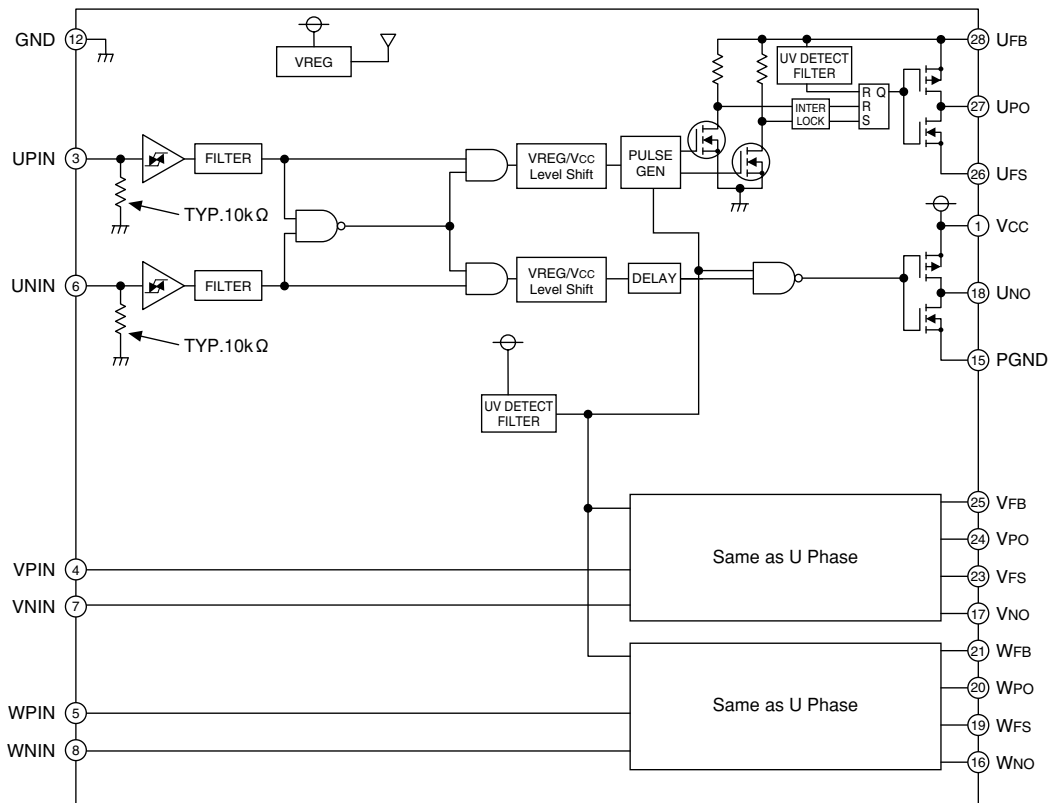
PIN CONFIGURATION (TOP VIEW)



NC:NO CONNECTION

Outline 28X9R

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified)

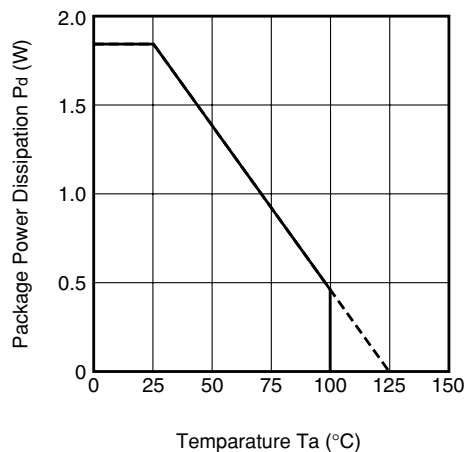
Symbol	Parameter	Conditions	Ratings	Unit
U,V,WFB	High Side Floating Supply Absolute Voltage		-0.5 ~ 624	V
U,V,WFS	High Side Floating Supply Offset Voltage		U,V,WFB-24 ~ U,V,WFB +0.5	V
VBS	High Side Floating Supply Voltage	VBS = *FB-*FS	-0.5~24	V
U,V,WPO	High Side Output Voltage		U,V,WFS-0.5 ~ U,V,WFB+0.5	V
VCC	Low Side Fixed Supply Voltage		-0.5~24	V
U,V,WNO	Low Side Output Voltage	*PIN, *NIN Terminal	-0.5~VCC+0.5	V
U,V,WIN	Logic Input Voltage		-0.5~VCC+0.5	V
dVS/dt	Allowable Offset Supply Voltage Transient	Ta = 25°C, On Board	±50	V/ns
PD	Package Power Dissipation	Ta > 25°C, On Board	1.84	W
Kθ	Linear Derating Factor		18.4	mW/°C
Rth(j-c)	Junction-Case Thermal Resistance		54.39	°C/W
Tj	Junction Temperature		-20 ~ 125	°C
Topr	Operation Temperature		-20 ~ 100	°C
Tstg	Storage Temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
U,V,WFB	High Side Floating Supply Absolute Voltage		Vs+10	—	Vs+20	V
U,V,WFS	High Side Floating Supply Offset Voltage		0	—	500	V
VBS	High Side Floating Supply Voltage	VBS = *FB-*FS	10	—	20	V
VCC	Low Side Fixed Supply Voltage		10	—	20	V
VIN	Logic Input Voltage	*PIN, *NIN Terminal	0	—	5	V
VPND	Power GND		-5	—	5	V

* For proper operation, the device should be used within the recommend conditions.

THERMAL DERATING FACTOR CHARACTERISTIC (MAXIMUM RATING)



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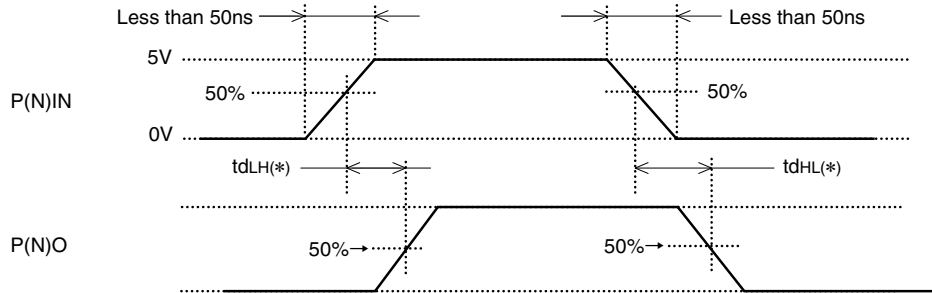
ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=Vbs(=*FB*FS)=15V unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
IFS	Floating Supply Leakage Current	V _B = V _S = 600V, 1 per phase	—	—	1.0	μA
I _{BS}	V _{BS} Standby Current	1 per phase	—	0.2	0.5	mA
I _{CC}	V _{CC} Standby Current		—	1.0	2.0	mA
V _{OH}	High Level Output Voltage	I _O = 0A, *NO, *PO	14.9	—	—	V
V _{OL}	Low Level Output Voltage	I _O = 0A, *NO, *PO	—	—	0.1	V
V _{IH}	High Level Input Threshold Voltage	*PIN, *NIN	2.7	—	—	V
V _{IL}	Low Level Input Threshold Voltage	*PIN, *NIN	—	—	0.8	V
I _{IH}	High Level Input Bias Current	*PIN, *NIN = 5V	0.3	0.5	1.0	mA
I _{IL}	Low Level Input Bias Current	*PIN, *NIN = 0V	—	0	—	μA
V _{BSuvr}	V _{BS} Supply UV Reset Voltage		7.5	8.5	9.5	V
V _{BSuvh}	V _{BS} Supply UV Hysteresis Voltage		0.2	0.5	0.8	V
t _{VBSuv}	V _{BS} Supply UV Filter Time		—	7.5	—	μs
V _{CCuvr}	V _{CC} Supply UV Reset Voltage		7.5	8.5	9.5	V
V _{CCuvh}	V _{CC} Supply UV Hysteresis Voltage		0.2	0.5	0.8	V
t _{VCCuv}	V _{CC} Supply UV Filter Time		—	7.5	—	μs
I _{OH}	Output High Level Short Circuit Pulsed Current	*PO, *NO = 0V, *PIN, *NIN = 5V, PW < 10 μs	120	200	—	mA
I _{OL}	Output Low Level Short Circuit Pulsed Current	*PO, *NO = 15V, *PIN, *NIN = 0V, PW < 10 μs	350	500	—	mA
R _{OH}	Output High Level On Resistance	I _O = 20mA, R _{OH} = (V _{OH} -V _O) /20mA	—	40	70	Ω
R _{OL}	Output Low Level On Resistance	I _O = 20mA, R _{OL} = V _O /20mA	—	15	30	Ω
tdLH(HO)	High Side Turn-On Propagation Delay	CL = 1000pF between *HO-*Vs Note.1	340	650	855	ns
tdHL(HO)	High Side Turn-Off Propagation Delay	CL = 1000pF between *HO-*Vs Note.1	340	650	855	ns
trH	High Side Turn-On Rise Time	CL = 1000pF between *HO-*Vs Note.2	20	130	220	ns
tfH	High Side Turn-Off Fall Time	CL = 1000pF between *HO-*Vs Note.2	—	50	75	ns
tdLH(LO)	Low Side Turn-On Propagation Delay	CL = 1000pF between *LO-PGND Note.1	340	650	855	ns
tdHL(LO)	Low Side Turn-Off Propagation Delay	CL = 1000pF between *LO-PGND Note.1	340	650	855	ns
trL	Low Side Turn-On Rise Time	CL = 1000pF between *LO-PGND Note.2	20	100	200	ns
tfL	Low Side Turn-Off Fall Time	CL = 1000pF between *LO-PGND Note.2	—	50	75	ns
ΔtdLH	Delay Matching, High Side and Low Side Turn-On	tdLH (*HO) -tdLH (*LO)	—	—	50	ns
ΔtdHL	Delay Matching, High Side and Low Side Turn-Off	tdHL (*HO) -tdHL (*LO)	—	—	50	ns
t _{filter}	Input Filter Time	*PIN, *NIN : Convex Pulse	260	380	500	ns
		*PIN, *NIN : Concave Pulse	310	450	590	ns

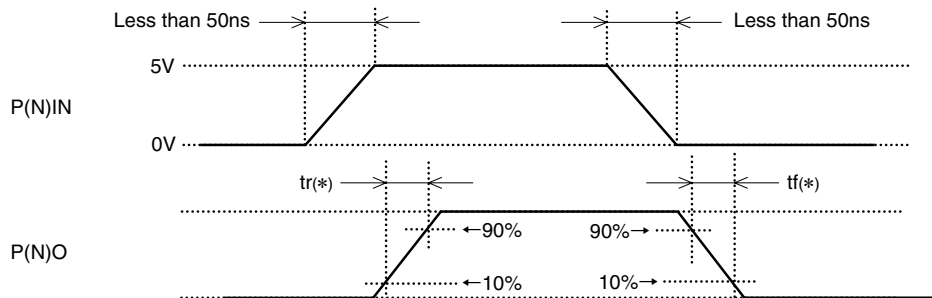
* Typ. is not specified.

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Note1 : Propagation Delay Timing (Output capacitor load CL = 1000pF).



Note2 : Output Rise/Fall Timing (Output capacitor load CL = 1000pF).



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FUNCTION TABLE

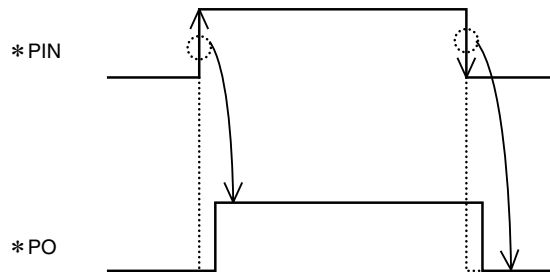
U,V,WPIN	U,V,WNIN	UV(VCC)	UV(VBS)	U,V,WPO	U,V,WNO	Behavioral state
H→L	L	H	H	L	L	*PO = L, *NO = L
H→L	H	H	H	L	H	*NO = H
L→H	L	H	H	H	L	*PO ON = H
L→H	H	X	H	L	L	*NO, *PO = L when *PIN, *NIN is "L" at the same time
X	L	H	L	L	L	*PO = L when Vbs UV tripped.
H→L	X	L	H	L	L	*NO = L when Vcc UV tripped.

Note1 : "L" state of Vbs UV, Vcc UV means that UV trip voltage.

2 : In the case of both input signals (*PIN and *NIN) are "H", output signals (*PO and *NO) become "L".

3 : X (*PIN) : L→H or H→L X (*HIN) : H or L.

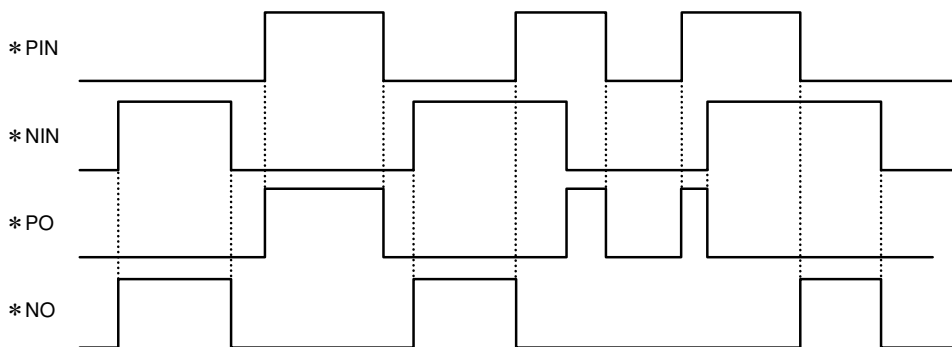
4 : Output Signal (*Po) is triggered by the edge of input signal.



TIMING DIAGRAM

1. Input/Output Timing Diagram

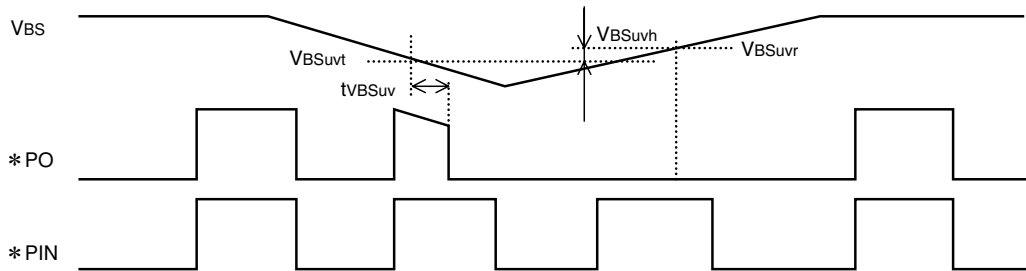
High Active, in the case of both input signals (*PIN, *NIN) are "H", output signals (*PO, *NO) become "L".



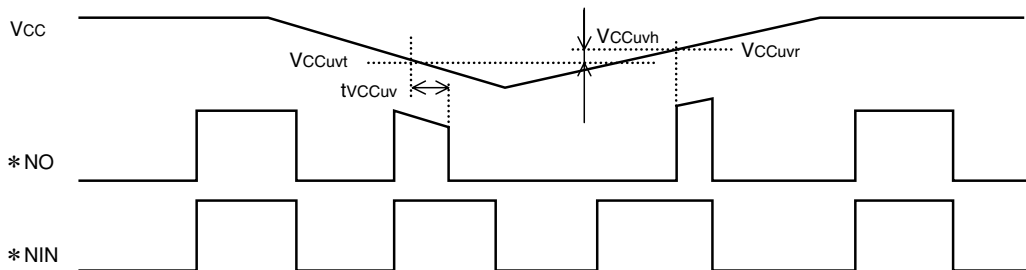
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2. Vcc (VBS) Supply Under Voltage Lockout Timing Diagram

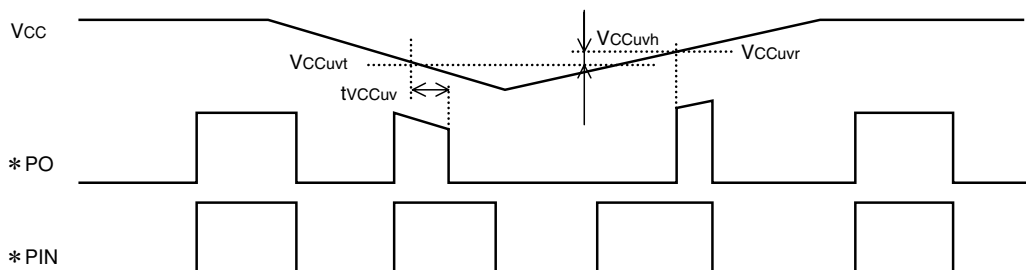
If V_{BS} supply voltage drops below UV trip voltage (V_{BSuvt}) for V_{BS} supply UV filter time, output signal is shut down. As soon as V_{BS} supply voltage rises over UV reset voltage, output signal *PO becomes "H" at following edge of input signal.



If V_{CC} supply voltage drops below UV trip voltage (V_{CCuvt}) for V_{CC} supply UV filter time, *NO output signal is shut down. As soon as V_{CC} supply voltage rises over UV reset voltage, output signal *NO becomes "H" if *NIN input signal is "H".



If V_{CC} supply voltage drops below UV trip voltage (V_{CCuvt}) for V_{CC} supply UV filter time, *PO output signal is shut down. As soon as V_{CC} supply voltage rises over UV reset voltage, output signal *PO becomes "H" if *PIN input signal is "H".



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3. Allowable Supply Voltage Transient

It is recommended to supply V_{CC} firstly and supply V_{BS} secondly. When shutting off supply voltage, please shut off V_{BS} firstly and shut off V_{CC} secondly. When applying V_{CC} and V_{BS} , power supply should be applied slowly. If it rises rapidly, output signal (HO or LO) may be malfunction.

PACKAGE OUTLINE

