

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

MITSUBISHI SEMICONDUCTOR <TRANSISTOR ARRAY>

# M63816P/FP/KP

8-UNIT 300mA TRANSISTOR ARRAY WITH CLAMP DIODE

## DESCRIPTION

M63816P/FP/KP are eight-circuit Single transistor arrays with clamping diodes. The circuits are made of NPN transistors. Both the semiconductor integrated circuits perform high-current driving with extremely low input-current supply.

## FEATURES

- Three package configurations (P, FP, and KP)
- Medium breakdown voltage ( $BV_{CEO} \geq 35V$ )
- Synchronizing current ( $I_{C(max)} = 300mA$ )
- With clamping diodes
- Low output saturation voltage
- Wide operating temperature range ( $T_a = -40$  to  $+85^\circ C$ )

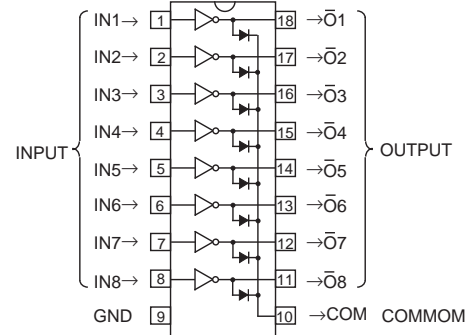
## APPLICATION

Driving of digit drives of indication elements (LEDs and lamps) with small signals

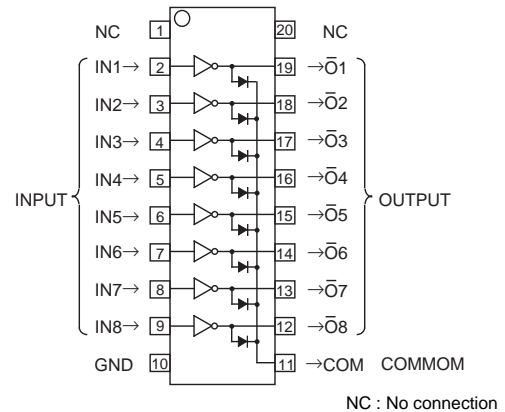
## FUNCTION

The M63816P/FP/KP each have eight circuits consisting of NPN transistor. A spike-killer clamping diode is provided between each output pin (collector) and COM pin. The transistor emitters are all connected to the GND pin. The transistors allow synchronous flow of 300mA collector current. A maximum of 35V voltage can be applied between the collector and emitter.

## PIN CONFIGURATION

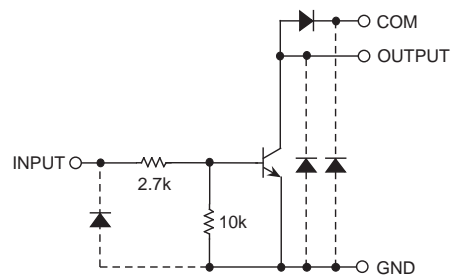


Package type 18P4G(P)



20P2N-A(FP)  
 Package type 20P2E-A(KP)

## CIRCUIT DIAGRAM



The eight circuits share the COM and GND.

The diode, indicated with the dotted line, is parasitic, and cannot be used.

Unit:  $\Omega$

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**ABSOLUTE MAXIMUM RATINGS** (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Conditions	Ratings	Unit	
V <sub>CEO</sub>	Collector-emitter voltage	Output, H	-0.5 ~ +35	V	
I <sub>C</sub>	Collector current	Current per circuit output, L	300	mA	
V <sub>I</sub>	Input voltage		-0.5 ~ +35	V	
I <sub>F</sub>	Clamping diode forward current		300	mA	
V <sub>R</sub>	Clamping diode reverse voltage		35	V	
P <sub>d</sub>	Power dissipation	Ta = 25°C, when mounted on board	M63816P	1.79	W
			M63816FP	1.10	
			M63816KP	0.68	
T <sub>opr</sub>	Operating temperature		-40 ~ +85	°C	
T <sub>stg</sub>	Storage temperature		-55 ~ +125	°C	

**RECOMMENDED OPERATING CONDITIONS** (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Test conditions	Limits			Unit	
			min	typ	max		
V <sub>O</sub>	Output voltage		0	—	35	V	
I <sub>C</sub>	Collector current (Current per 1 circuit when 8 circuits are coming on simultaneously)	M63816P	Duty Cycle no more than 50%	0	—	250	mA
			Duty Cycle no more than 100%	0	—	170	
		M63816FP	Duty Cycle no more than 30%	0	—	250	
			Duty Cycle no more than 100%	0	—	130	
		M63816KP	Duty Cycle no more than 12%	0	—	250	
			Duty Cycle no more than 100%	0	—	100	
V <sub>IN</sub>	Input voltage		0	—	20	V	

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, Ta = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
V (BR) CEO	Collector-emitter breakdown voltage	I <sub>CEO</sub> = 10μA	35	—	—	V
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	I <sub>IN</sub> = 1mA, I <sub>C</sub> = 10mA	—	—	0.2	V
		I <sub>IN</sub> = 2mA, I <sub>C</sub> = 150mA	—	—	0.8	
V <sub>IN(on)</sub>	"On" input voltage	I <sub>IN</sub> = 1mA, I <sub>C</sub> = 10mA	2.4	3.5	4.2	V
V <sub>F</sub>	Clamping diode forward voltage	I <sub>F</sub> = 250mA	—	1.2	2.0	V
I <sub>R</sub>	Clamping diode reverse current	V <sub>R</sub> = 35V	—	—	10	μA
h <sub>FE</sub>	DC amplification factor	V <sub>CE</sub> = 10V, I <sub>C</sub> = 10mA	50	—	—	—

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, Ta = 25°C)

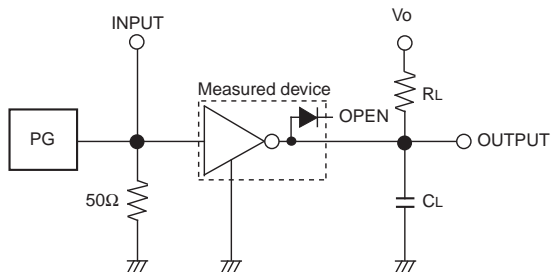
Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
t <sub>on</sub>	Turn-on time	C <sub>L</sub> = 15pF (note 1)	—	125	—	ns
t <sub>off</sub>	Turn-off time		—	250	—	ns

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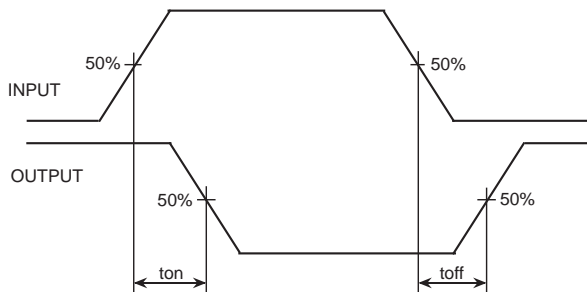
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**NOTE 1 TEST CIRCUIT**

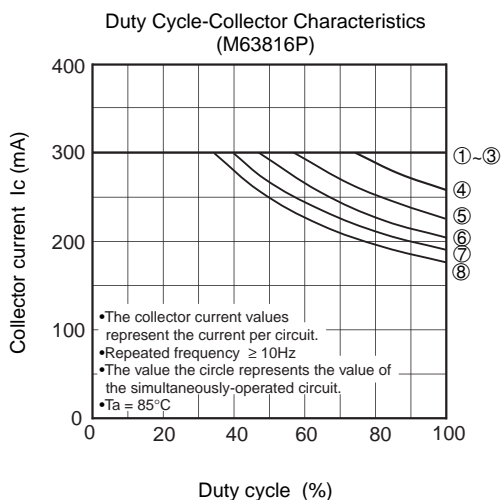
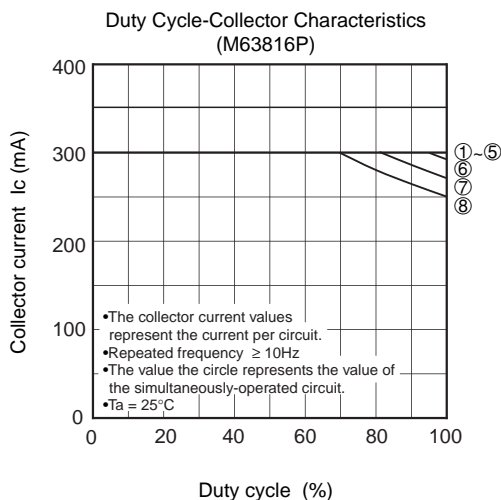
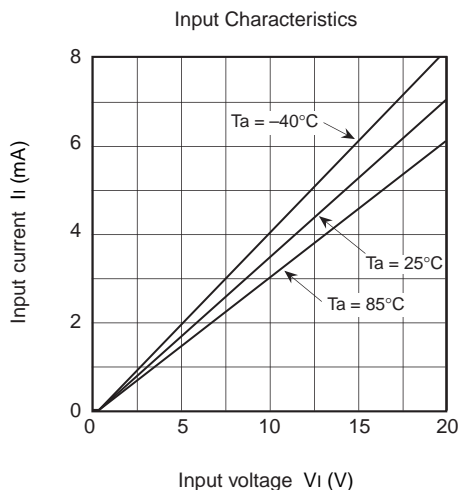
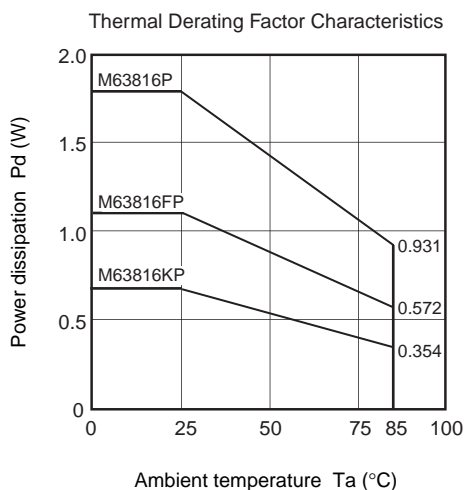


- (1) Pulse generator (PG) characteristics : PRR = 1kHz,  
 $t_w = 10\mu s$ ,  $t_r = 6ns$ ,  $t_f = 6ns$ ,  $Z_o = 50\Omega$ ,  $V_{IH} = 3V$
- (2) Input-output conditions :  $R_L = 220\Omega$ ,  $V_o = 35V$
- (3) Electrostatic capacity  $C_L$  includes floating capacitance at connections and input capacitance at probes

**TIMING DIAGRAM**



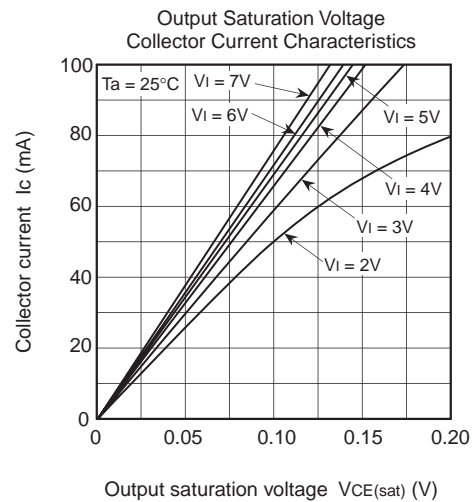
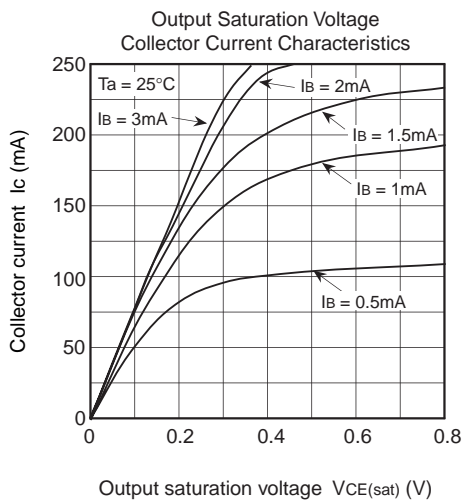
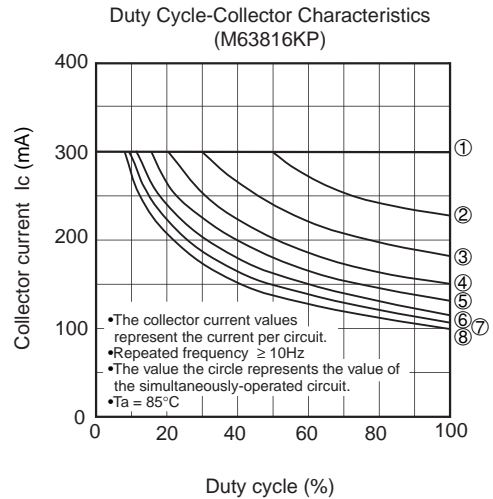
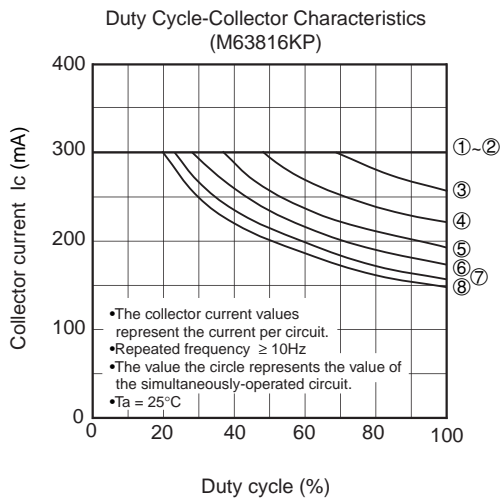
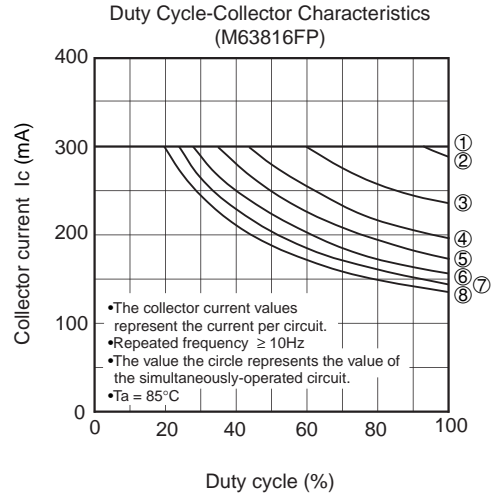
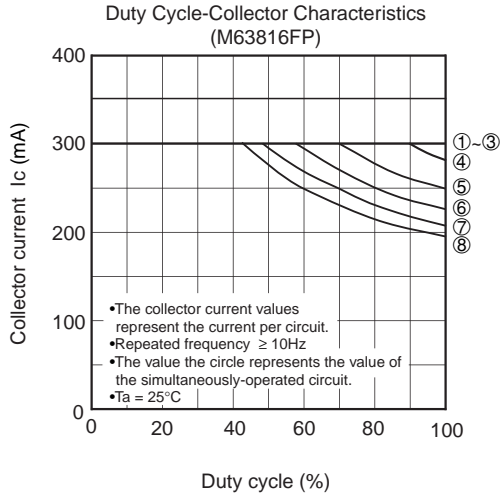
**TYPICAL CHARACTERISTICS**



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