

The C702 is a medium voltage, high current disc pack SCR employing a Bar gate, amplifying gate structure. This amplifying gate design allows the SCR to be reliably operated at high di/dt and high dv/dt conditions in phase control applications.

#### FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and  $I^2t$  Ratings

#### APPLICATIONS:

- DC Power Supplies
- Motor Controls
- AC Soft-Starters

#### ORDERING INFORMATION

Select the complete Part Number using the table below.  
 EXAMPLE: C702CB is a 3200V-1000A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating	Voltage Code	Current Rating
	$V_{DRM}$ - $V_{RRM}$		$I_{TAVG}$
<b>C702</b>	2400V	<b>LD</b>	1000A
	2600V	<b>LM</b>	
	2800V	<b>LN</b>	
	3000V	<b>CP</b>	
	3200V	<b>CB</b>	

**Absolute Maximum Ratings**

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	3200	Volts
Non-repetitive Transient Peak Reverse Voltage	$V_{RSM}$	$V_{RRM} + 100$	Volts
Average On-State Current, $T_C=74^\circ\text{C}$	$I_{T(Avg.)}$	1000	A
RMS On-State Current, $T_C=74^\circ\text{C}$	$I_{T(RMS)}$	1571	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	1220	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	1916	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	$I_{TSM}$	21,500	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	$I_{TSM}$	20,500	A
Fuse Coordination $I^2t$ , 60Hz	$I^2t$	1.93E+06	$A^2s$
Fuse Coordination $I^2t$ , 50Hz	$I^2t$	2.10E+06	$A^2s$
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	$P_{GM}$	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	$T_j$	-40 to+125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^\circ\text{C}$
Approximate Weight		1	lb
		0.45	Kg
Mounting Force		5500-6000	lbs
		24.5 - 26.7	Knewtons

**Electrical Characteristics, Tj=25°C unless otherwise specified**

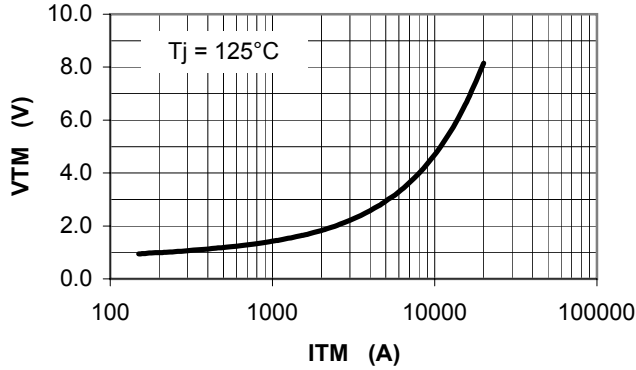
Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	$I_{DRM}$	Tj=125°C, $V_{DRM}$ =Rated			150	ma
Repetitive Peak Reverse Leakage Current	$I_{RRM}$	Tj=125°C, $V_{RRM}$ =Rated			150	ma
Peak On-State Voltage	$V_{TM}$	Tj=125°C, $I_{TM}$ =2000A			1.85	V
$V_{TM}$ Model, Low Level	$V_0$	Tj=125°C			0.944	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - \pi \cdot I_{TM}$			4.25E-04	$\Omega$
$V_{TM}$ Model, High Level	$V_0$	Tj=125°C			1.18	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			3.49E-04	$\Omega$
$V_{TM}$ Model, 4-Term	A	Tj=125°C			0.363	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			0.108	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				3.42E-04	
	D				-8.33E-04	
Turn-On Delay Time	$t_d$	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20V		2.5		us
Turn-Off Time	$t_q$	Tj=125°C $dv/dt = 20V/us$ to 80% $V_{DRM}$		400		us
$dv/dt_{(crit)}$	$dv/dt$	Tj=125°C Exp. Waveform $V_D = 80\%$ Rated	400			V/us
Gate Trigger Current	$I_{GT}$	Tj=25°C $V_D = 12V$	30	100	200	ma
Gate Trigger Voltage	$V_{GT}$		0.8	2.0	4.5	V
Peak Reverse Gate Voltage	$V_{GRM}$				5	V

**Thermal Characteristics**

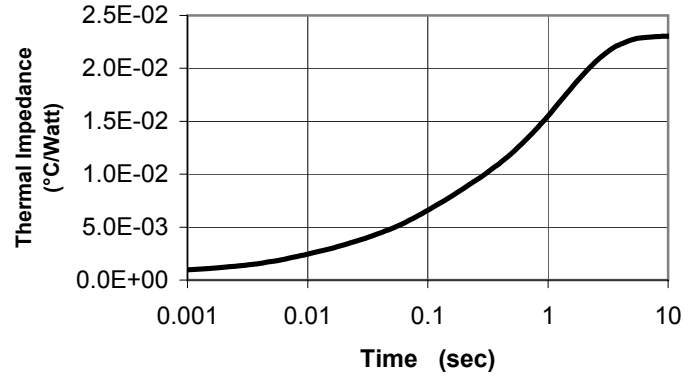
Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	$R\theta_{jc}$	Double side cooled		0.021	0.023	°C/Watt
Case to Sink	$R\theta_{cs}$	Double side cooled		0.004	0.006	°C/Watt

Thermal Impedance Model	$Z\theta_{jc}$	Double side cooled	min	typ	max	Units	
$Z\theta_{jc}(t) = \sum(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$		where:	N =	1	2	3	4
			A(N) =	7.26E-04	1.58E-03	4.55E-03	1.62E-02
			Tau(N) =	4.49E-05	8.21E-03	8.84E-02	1.31E+00

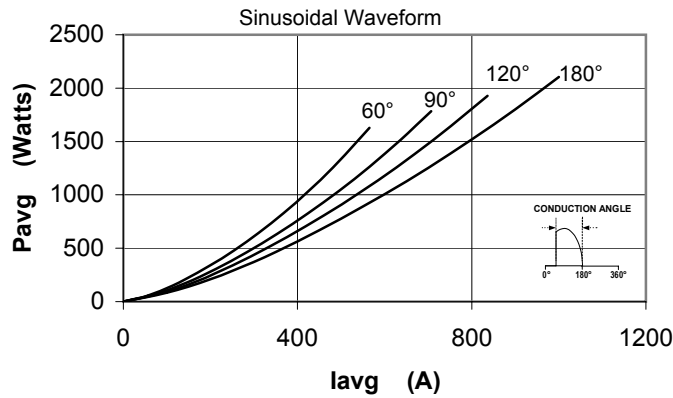
**Maximum On-State Voltage Drop**



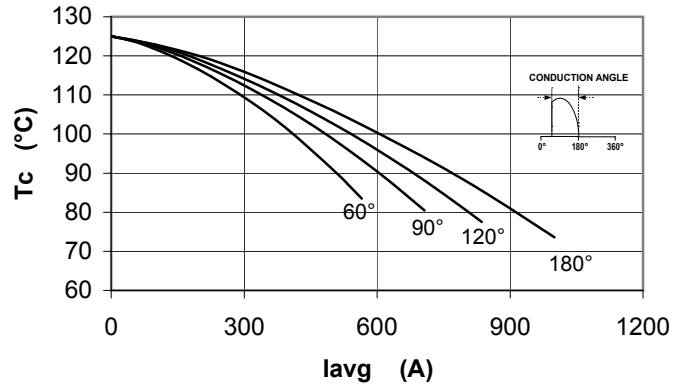
**MAXIMUM TRANSIENT THERMAL IMPEDANCE**



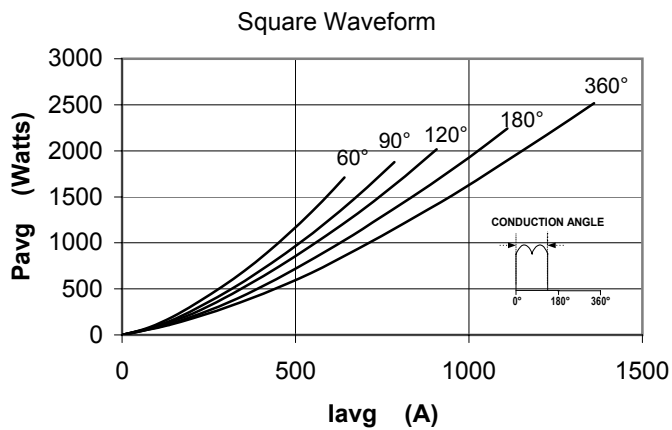
**Maximum On-State Power Dissipation**



**Maximum Allowable Case Temperature**  
Sinusoidal Waveform



**Maximum On-State Power Dissipation**



**Maximum Allowable Case Temperature**  
Square Waveform

